1991

Large signal modeling and characterization of hererojunction bipolar transistors

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LARGE SIGNAL MODELING AND CHARACTERIZATION OF HETEROJUNCTION BIPOLAR TRANSISTORS

by

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A Thesis
Presented to the Graduate Committee
of Lehigh University
in Candidacy for the Degree of
Master of Science
in
Electrical Engineering

Lehigh University
May 1991

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MEMORANDUM

TO: Bruce Correll, Registrar

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SUBJECT: Approved master's thesis

We have received a properly approved master's thesis in Electrical Engineering from David Scott Whitefield.

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This thesis is accepted and approved in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering.

May 9, 1991
Date

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ACKNOWLEDGEMENTS

I am grateful to my advisor, Dr. James C.M. Hwang, for his expert guidance and support over the course of this work. I would also like to thank Dr. C.J. Wei and Bill Melvin for all their help in the lab.

I extend my love and appreciation to my family, and to Lynne for their encouragement and support, and for understanding when I had to work.

Finally, I gratefully acknowledge the Air Force for allowing me to attend graduate school, and the Air Force Office of Scientific Research for funding this project.

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ABSTRACT

Because of their high gain and wide bandwidth, heterojunction bipolar transistors (HBTs) are excellent for use in high speed microwave and digital circuits . In this work, large-signal characterization and modeling is performed to facilitate their use in high power amplifier circuits. DC to 40GHz characterization is performed on HBTs of various designs and sizes. Pulsed and thermal measurements are also performed to determine the junction temperature and its effects on device characteristics. A ten-element equivalent circuit model is proposed in which only three elements are allowed to vary with bias. This equivalent circuit model can simulate the bias range with less than 2% mean square error.

1. INTRODUCTION

The heterojunction bipolar transistor (HBT) is an excellent device for microwave power applications. It is capable of higher current density and lower leakage current than the metal semiconductor field effect transistor (MESFET), making the HBT more efficient for high power applications. HBTs capable of 5 Watts per millimeter of emitter length with 68% efficiency have been reported [1]. The HBT also has a higher bandwidth than traditional silicon bipolar transistors, with current HBTs having unity power gain cutoff frequencies of 100-200GHz [2]. To take advantage of the power handling capability of the HBT in monolithic microwave integrated circuits (MMICs), it is necessary to analyze the large-signal characteristics of the HBT and to develop an accurate and efficient equivalent circuit model to aid in circuit design.

This work begins with a brief background description of the basic HBT structure and its theoretical operation, followed by an in-depth description of characterization results for specific HBT structures. Results of pulsed DC and elevated temperature measurements are analyzed to determine the thermal effects on HBTs at high power levels. Finally a nonlinear equivalent circuit model is presented which is based on DC and S-parameter data at many bias conditions.

2. THEORY OF TRANSISTOR OPERATION

HBTs are bipolar transistors where at least one p-n junction is a heterojunction between two semiconductors possessing different bandgaps. The basic concept of an HBT is to use band gap variations in addition to electric fields to control the movement of electrons and holes independently.

The initial concept of an HBT was conceived by Shokley and patented in 1951 but no devices were fabricated due to the inadequacy of semiconductor growth technology. Not until the mid-70s has the growth of heterojunction material been possible with the advent of molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD).

Figure 1 shows an energy-band diagram of an AlGaAs/GaAs HBT. The emitter is AlGaAs which has a wider bandgap than the base (GaAs). The conduction band spike between the emitter and base is due to the heterojunction and can be virtually eliminated with gradual composition grading. Therefore, the change in bandgap has the greatest effect on the valence band, causing the electrons and holes to see different barrier heights. From Figure 1, the HBT current gain, β, and maximum gain, β_{max}, are given by the expression:

$$\beta = \left(\frac{I_C}{I_B}\right) = \left(\frac{I_n - I_r}{I_p + I_r + I_s}\right) < \left(\frac{I_n}{I_p}\right) = \beta_{max} \qquad (1)$$

Using the expressions for I_n and I_p,

$$I_n = (Area)\, N_d \nu_{nb} \exp\left(\frac{-qV_b}{kT}\right) \tag{2}$$

$$I_p = (Area)\, N_a \nu_{pe} \exp\left(\frac{-q(V_b + \Delta E_G)}{kT}\right) \tag{3}$$

a final expression for β_{max} can be derived:

$$\beta_{max} = \left(\frac{N_d \nu_{nb}}{N_a \nu_{pe}}\right) \exp\left(\frac{\Delta E_G}{kT}\right) \tag{4}$$

where ν_{nb} and ν_{pe} are mean speeds due to drift and diffusion effects, ΔE_G is the bandgap difference and N_a and N_d are the base and emitter doping concentrations [3,4,5].

The traditional homojunction bipolar transistor has $\Delta E_G = 0$, therefore to increase β_{max}, the emitter doping must be much greater than the base doping as seen in Equation (4). Given the same doping concentrations, an HBT with the bandgap difference between GaAs and $Al_{0.3}Ga_{0.7}As$ of 10 to 15kT, can have a β_{max} 50 to 100 times greater. Such large β values are not necessary for most applications which means β may be reduced by doping the base orders of magnitude higher than the emitter. This doping change reduces base resistance and transit times and also reduces the emitter capacitance, thus increasing the maximum frequency of operation.

Figure 2 shows the cross-section of a typical HBT with a wide bandgap emitter epitaxially grown on the base and collector layers. Since the HBT is a vertical device, the critical vertical dimensions and junction grading features can be controlled to one

atomic layer. In addition, horizontal dimensions for the HBT are not as critical and currently state-of-the-art devices do not require sub-micron lithography.

3. DC CHARACTERIZATION

DC measurements determine the most basic device parameters and provide insight into device physics. These measurements are also used to select high performance devices, define regions of operation for subsequent RF measurements, and serve as a starting point for determining RF equivalent circuit parameters. All measurements were performed on-wafer which eliminates the substrate thinning, dicing and packaging steps and allows for rapid characterization of many devices. On-wafer measurements however, cause the test devices to become hotter than packaged ones inducing undesirable thermal effects. HBT samples were obtained from the Air Force Wright Laboratory [6] and had single 1μ x 8μ emitters. These devices were fabricated on 625μ thick GaAs semi-insulating substrates.

3.1 DC measurement set up

The DC equipment used in this work includes an HP4142 Semiconductor Parametric Analyzer equipped with three source and monitoring units of either voltages or currents. These units are connected to shielded DC probes mounted on an Alessi probe station. Five probes are used for most measurements, one for ground and a pair of probes for each signal path, one sourcing and one monitoring. All measurements are controlled from a PC computer where the data is stored.

3.2 Common emitter characteristics

The common emitter current-voltage (I-V) characteristics of the single emitter HBT are shown in Figure 3. Several features of this characteristic are unique to the HBT. First, there is the large offset voltage. In general, this offset ranges from 0 to 0.4V depending on the structure and is caused by the nonsymmetric nature of the base-emitter heterojunction and base-collector homojunction. Specifically, the offset voltage is due to the difference between the turn on voltages and junction areas of the base-emitter and base-collector junctions, and any base-emitter energy bandgap spike [7,8,9]. Below the turn on voltage, all the base current is injected into the collector with unity reverse gain.

In the forward-active region, the common emitter response shows a negative resistance behavior at high power levels. This is due to thermal effects and will be discussed further in Chapter 4. Due to the heterojunction, the gain of an HBT decreases with increasing temperature [10] which is the opposite behavior of a homojunction transistor. Due to the thermal effects, the output resistance in the forward-active region is obscured. However, this resistance can be easily obtained from high frequency S-parameter measurements as described in Chapter 4. Since the base can be highly doped, base-width modulation effects are minimized and the output resistance can be more than an order of magnitude higher than in silicon bipolar transistors [11]. Figure 3 also shows that the DC gain of this particular transistor is $\beta = 13$ -- in this work, the microwave transistors had β values in the range from 5 to 15, with most below 10. These gains are typical for microwave power devices.

For modeling purposes, the parameters that are derived from the common emitter characteristics include turn-on voltage, β and breakdown voltage. The sum of the series collector and emitter resistance can also be extracted from the slope of the rising collector current in the saturation region.

3.3 Base and collector current characteristics

Figure 4 is a typical Gummel plot showing base and collector currents versus the base-emitter voltage. These currents essentially follow the diode equation:

$$I = I_s \exp\left(\frac{V_F}{nV_T}\right) \tag{5}$$

where I_s is the saturation current. V_F is the forward-voltage across the intrinsic base-emitter junction, which is the applied V_{be} minus the drop across the parasitic emitter and base resistances. The ideality factor, n, describes the slope (on log axes) of the ideal characteristics and V_T is the thermal voltage kT/q. The saturation behavior of I_b and I_c at high current levels is caused by the increased voltage drop across the parasitic base and emitter resistances.

For modeling purposes, many parameters derived from the Gummel plot are used including I_s and n , the collector saturation current and ideality factor, I_{se} and ne, the base saturation current and ideality factor, and Rb and Re the base and emitter parasitic resistances. Also, the behavior of β versus V_{be} can be analyzed as shown in Figure 5. This figure shows the typical reduction of β at low and high currents which is an important factor for large-signal modeling and will be discussed in Chapter 6.

4. RF CHARACTERIZATION

The goal of this work is to develop a high frequency equivalent circuit model of the HBT. Therefore, high frequency RF measurements are essential for model development and comparison. The interpretation of S-parameters is the most useful method to characterize a device at microwave frequencies and is used extensively in this work. The S-parameters S11 and S22 are the input and output reflection coefficients, giving the input and output complex impedance. S21 and S12 are the forward and reverse transmission coefficients. From the four S-parameters, all other parameters such as Z, Y, and H-parameters can be readily derived [12].

The most popular figures of merit for characterizing the high frequency limits of a device include H21, the forward current gain, and its unity gain frequency, f_T. Also used are the power gains MAG and MSG, maximum available gain and maximum stable gain. At low frequencies, the power gain is unconditionally stable (MAG), and at higher frequencies, the power gain becomes stable only for specific impedance matching conditions (MSG). The unity gain frequency for power gain is f_{max}.

4.1 RF measurement set up

The equipment used to measure S-parameters includes the HP8510-B, a 40GHz network analyzer with a two port S-parameter test-set. The network analyzer is capable of accurate S-parameter calibrations and measurements up to 40GHz. All RF measurements are made on-wafer with two Tektronix 40GHz RF probes mounted on

an Alessi probe station, and the DC bias during high frequency measurements is supplied by the HP4142 semiconductor parametric analyzer. All the equipment is controlled by a PC computer running the EEsof network analyzer control software, Anacat [13].

The Tektronix RF probes are highly precise and delicate instruments. They contain an adapter from 2.4mm coaxial cable to a coplanar waveguide fabricated on a ceramic substrate. The waveguide is in a ground-signal-ground configuration and is terminated at the tip of the probe in three nickel contact pads, see Figure 6. The devices under test are fabricated with contact pads in the same ground-signal-ground configuration with 125μm pitch.

4.2 Calibration

Because of the high frequencies involved, the RF measurement system must be calibrated each time the RF probes are reconnected. This calibration is a many-stepped process involving numerous touch-downs of the probes and considerable computer calculations. A successful calibration will correct for all phase shifts, reflections and losses from the point of measurement inside the network analyzer to the reference planes at the tips of both probes.

The first step in calibrating the on-wafer measurement system is to planarize the RF probes to the surface of the test wafer. If all three pads of both probes are not touching the device, large looping errors in the S-parameter data will be produced.

The second step of the process is to calibrate the network analyzer. A Tektronix

CAL 96 calibration wafer is used for this purpose. This sapphire wafer contains laser-trimmed calibration standards including a short circuit, a through-line and a 50Ω load (see Figure 7). Calibration consists of taking S-parameter measurements over the full frequency range of interest while both probes are separately contacted to the wafer to create the following electrical conditions:

1) A short circuit: The ground-signal-ground pads of each probe are contacted to a simple strip of metallization.

2) An open circuit: Each probe is rested on the bare sapphire insulation.

3) A matched load impedance: The calibration pattern creates a 50Ω resistive load between the signal pad and the two ground pads of the probe.

4) A through line: The two probes are placed very close to each other and contacted to a pattern of three metallization strips. The signal of one probe is directly connected to the signal of the other probe. Likewise, the ground pads of each probe are connected together.

Once all calibration measurements are performed, the network analyzer computes a set of twelve error coefficients for each measurement frequency. For all subsequent measurements, these coefficients are applied to the raw S-parameter data to filter out effects from the probes, connectors and cables. This filtering results in S-parameters which accurately characterize the device under test. Verification patterns are also supplied on the sapphire wafer to verify an accurate calibration.

4.3 S-parameter measurement results

S-parameter measurements from 0.5 to 40GHz have been performed for three HBT devices under various bias conditions. Figure 8 and Figure 9 show a representative set of S-parameters. S11 and S22 are displayed on a Smith chart and show an input and output impedance that is basically capacitive. The real part of the input impedance ranges from 500Ω at 0.5GHz to 35Ω at 40GHz. The real part of the output ranges from several megaohms at 0.5GHz to 35Ω at 40GHz. In Figure 9, the magnitude of S21 and S12 are shown versus frequency. The forward gain, S12, is seen to decrease from a maximum of 6dB while the reverse gain, S21, increases from -40dB to -15dB.

Figure 10 illustrates the magnitude of the forward current gain, $|H21|$, and the power gain with their respective cutoff frequencies essentially equal, i.e., $f_T = f_{max} =$ 33GHz for this particular transistor. The HBTs measured had values of f_T ranging from 30 to 50GHz and f_{max} values ranging from 15 to 35GHz.

For equivalent circuit modeling purposes it is important to measure all four S-parameters over the full range of operating conditions. Figure 11 shows the chosen bias points from the transistor saturation region to cutoff. Figure 12 shows a plot of $|H21|$ for several bias conditions. $|H21|$ can be seen to drop off at both high (bias point 6) and low currents (bias point 1). This nonlinear gain reduction is an important feature of the equivalent circuit model described in Chapter 7. f_T is seen to change with bias, especially near cur-off. This behavior is expected from the dependence of depletion region capacitance on bias at both the base-emitter and base-collector junctions.

5. PULSED DC MEASUREMENTS:

Semiconductor devices operated at high power levels are subject to many thermal effects which degrade performance. In homojunction transistors, thermal effects result in an increase in gain with increasing junction temperature leading to thermal runaway. Conversely for the HBT, thermal effects result in a reduction of gain with increasing temperature actually controlling device overheating. However, the reduction of *any* thermal effect is the most desirable and efficient heat-sinking is applied when devices are packaged. For proper heat sinking, the device substrate is thinned from about 625μ to 100μ and a plated metal heat-sink is applied [14,15].

For on-wafer measurements even at moderate power levels, un-packaged and un-thinned HBTs exhibit significant thermal effects. To analyze the thermal effects and simulate packaged device performance, pulsed DC measurements have been performed to reduce the average power hence junction temperature.

Figure 13 shows the measurement configuration where a pulsed base voltage is adjusted to obtain a desired base current. The average HBT base current is measured through R_{Diff} and the average collector current is measured through V_c. C_c supplies the current pulse to the collector while keeping the voltage fixed. R_1 and R_2 are added to reduce reflections and R_e allows monitoring of the emitter current waveform through an oscilloscope. The voltage waveform is such that the actual V_{be} of the transistor never reaches zero. This eliminates base current oscillations due to a hard turn off while supplying essentially zero power to the transistor. To further stabilize the

measurement, local grounding near the probe tips was found to be important as shown in Figure 14.

For the particular HBTs measured, an average thermal time constant of 5μs was found. At pulse widths of 1μs, thermal effects were found to be negligible, so actual pulsed I-V data was taken at this pulse width. A duty cycle of 1/2 was used, which reduces the total power through the device by 1/2. Figure 15 shows the common emitter I-V characteristics of the single 1μ x 8μ emitter HBT on a 625μ substrate. For this configuration, the pulsed measurement significantly reduced the thermal effects.

6. THERMAL MEASUREMENTS

It is important to obtain the emitter-base junction temperature for a range of power levels to fully quantify the thermal effects of the HBT. The base emitter voltage (V_{be}) is used as a temperature reference because at a constant base current, V_{be} is a function of temperature. The dependence of V_{be} on temperature is obtained empirically and used to find the junction temperature during normal operation. This temperature dependence is compared to theoretical calculations and found to be accurate.

To obtain the temperature dependence of V_{be}, several low power I-V measurements were performed on a device heated to a variety of known temperatures from 27°C to 190°C. These calibration measurements were performed on the device mounted in a metal TO-package which was connected to a Teflon test fixture and placed in an oven. Figure 16 shows the base current characteristics at the different ambient temperatures. In order to perform these measurements, the transistor was operated at a constant finite power level which produced a junction temperature slightly above the ambient and will have to be accounted for in the final analysis.

From the base current characteristics, Figure 17 shows the essentially linear dependence of V_{be} on junction temperature for a constant base current. This dependence is used to find the junction temperature of the device operated at different power levels in a room temperature ambient. A common emitter measurement is taken with I_b=4mA while V_{be} is monitored as a function of power. The junction temperature for each power level is calculated from V_{be}. As mentioned earlier, this calculation must

be adjusted due to the non-zero power used for the calibration measurements. Figure 18 shows the device junction temperatures, where the measured behavior is calibrated to predict a room temperature junction at zero power. The resulting thermal resistance is 1700°C/W.

This thermal resistance from the temperature measurements is compared with a three-dimensional heat flow analysis [16]. The geometry of the chip and transistor are approximated as shown in Figure 19. A and F are the chip width and thickness, and C and D are the transistor emitter dimensions. The emitter is generating heat which is dissipated through the bottom of the chip held at room temperature. All other chip surfaces are assumed adiabatic.

The exact solution of this heat flow is formulated in terms of infinite sums, and evaluated up to three digit accuracy. Because the actual transistor is not in the center of the chip, the correct dimension to use for chip width is uncertain. A maximum and minimum dimension were chosen, and the resulting range of possible temperatures are shown in Figure 20. The previous calibrated junction temperature values are seen to fall well within the range of this heat flow analysis.

From the determined junction temperature, the change in current gain, β, is shown in Figure 21 to be a approximately a linear function of temperature. The gain is reduced almost 10% at a junction temperature of 150°C.

7. BIAS-DEPENDENT EQUIVALENT CIRCUIT MODELING

Based on the many types of measurements described earlier, a high frequency equivalent circuit model of the HBT is developed. Modeling of discrete power devices at microwave frequencies is never trivial, and the nonlinearity of the HBT further complicates the task. Therefore this work concentrates on the nonlinearity in intrinsic device characteristics, while assuming parasitic elements behave linearly. The approach taken is to propose a simple microwave equivalent circuit in which several elements are permitted to vary with bias. The goal is to identify element values that vary significantly with bias which is critical to the HBT large-signal behavior.

7.1 Computer modeling tools

The CAD tools used for the modeling include HSPICE [17] a SPICE derivative capable of extracting bipolar junction transistor parameters from DC data. The LIBRA circuit simulator [18] is a powerful microwave equivalent circuit simulator and is used to perform the bulk of the modeling work. Unlike in SPICE, computations in LIBRA are performed in the frequency domain to yield fast and accurate steady state responses. A feature used extensively in this work is the capability of LIBRA to fine tune (optimize) a circuit to better fit measured S-parameter data. Unfortunately, a circuit with many elements will have many optimum solutions, so the determination of physically meaningful initial element values is very important for accurate results.

7.2 Bias dependent equivalent circuit model

Figure 22 shows the proposed microwave equivalent circuit model. For a particular device, a complete DC analysis is performed, and S-parameter measurements are taken at more than ten DC bias points in the forward-active region, shown in Figure 11. Initial model values are extracted from DC and RF data as described below.

7.3 Initial model element values

HSPICE is used to extract many starting element values from Gummel plots of base and collector currents and from common emitter characteristics. The parasitic resistances Rb and Re are extracted from Gummel plot data at high current levels. Approximate values of Rc and Rcb can be extracted from the common emitter saturation characteristics.

From RF characterization, a starting value of Ccb can be obtained from the well known approximate expression for the measured value f_{max}:

$$f_{max} = \sqrt{\frac{f_T}{8\pi R_b C_{cb}}} \tag{6}$$

Ro and Cce are estimated from the output reflection coefficient S22. Ceb is estimated from the base emitter junction area and the doping levels at the junction. A starting value of Ceb=1pF was used for the 1μ x 8μ devices.

From these initial values the equivalent circuit was optimized to fit S-parameter data at the many bias conditions allowing all elements to be optimized. This was performed to three devices to determine which element values were most sensitive to

changes in bias conditions.

Figure 23 shows the relative change of each element with bias. From this experiment it is apparent that the large-signal behavior is dominated by the change of Ceb, Reb, and β, therefore the final model is one in which all elements are held constant except for these three. The fixed elements are assigned the average value from the sensitivity analysis above. The final model with the fixed element values is shown in Figure 26.

7.4 Nonlinear behavior of elements

Starting all from the same model elements, the circuit is optimized separately for each bias condition allowing only Ceb, Reb, and β to vary. The result is a set of data for these three elements versus the different bias conditions, or the large-signal behavior of these elements. Figure 24 is a combined graph of these three elements versus the collector current bias. The expected nonlinear behavior of Ceb and Reb is apparent, and the typical β reduction at high and low current levels is seen. The increasing and decreasing behavior of Ceb and Reb are consistent with bipolar theory [19], and are fit very well by the exponential expressions:

$$R_{eb}=K_r\exp\left(\frac{I_c}{-n_r}\right) \tag{7}$$

$$C_{eb}=K_c\exp\left(\frac{I_c}{+n_c}\right). \tag{8}$$

7.5 Deviation from measurement

A representative plot of modeled and measured data is shown in Figure 25. Agreement is very good over the entire frequency range. To quantify the difference between the modeled and measured S-parameters a mean squared error calculation was performed [20]. At each bias condition this error was calculated for all S-parameters (real and imaginary parts) at all measured frequency values. The resultant mean squared error for all bias points is below two percent.

Additional variations with this model were performed where different numbers of elements were allowed to vary with bias while the rest were held constant. When four elements were allowed to vary (Reb, Ceb, β, and Rcb), the resulting error from measured data was very similar to the three element case described above. The two element case (Reb and Ceb varied, and β held constant) showed only slightly more error. When only one element was allowed to vary (Reb and Ceb separately) the errors were greater by orders of magnitude. Figure 27 shows the percent mean square error for all four cases.

The model with three bias-dependent elements is believed to be the most useful in terms of accuracy, efficiency, and versatility. Even though the two element model has sufficient accuracy, the addition of β as a nonlinear element is important because HBTs of different design have exhibited very different β behaviors.

8. FUTURE WORK

Work will continue on this large-signal modeling effort to relate the bias-dependence of model elements to the large-signal microwave response. Actual large-signal microwave measurements will be taken, and currently a pulsed technique is being developed. The model will be compared and modified based on the measured results.

Further DC pulsed measurements will be performed with duty cycles less than one half and pulse widths less than $1\mu s$ to ensure that the pulsed power is not raising the junction temperature significantly. These tests may require a manual technique using an oscilloscope or a curve tracer. Additional thermal measurements are also required to include higher temperature measurements, and to reduce power during these measurements. A pulsed technique will be used where the junction is first self-heated at normal operating conditions, then the junction temperature is measured by a short lower power pulse. From these measurements, a knowledge of the junction temperature at any DC bias condition can be obtained, as well as the junction temperature within the large-signal RF voltage swing. With accurate knowledge of the junction temperature during operating conditions, modeling of the thermal effects of the HBT can be achieved. This model will be incorporated into the overall large-signal model. To test its versatility, model results will be compared to devices of varying size and physical structure. Devices with thinned substrates will also be tested to verify thermal model predictions.

9. CONCLUSIONS

A simple yet accurate ten-element equivalent circuit model has been developed for the HBT. The model has seven fixed elements and three bias-dependent elements which vary in a nonlinear fashion. All three elements vary with elementary functions making them efficient for simulations; two are simple exponentials while the third is an inverted "U". The model is compared to measured S-parameter data with less than 2% mean square error.

Extensive DC and RF characterization has been performed for evaluation of device performance and extraction of model elements. Pulsed DC and high temperature measurements have also been performed to analyze the thermal resistance and relate actual junction temperature to device performance.

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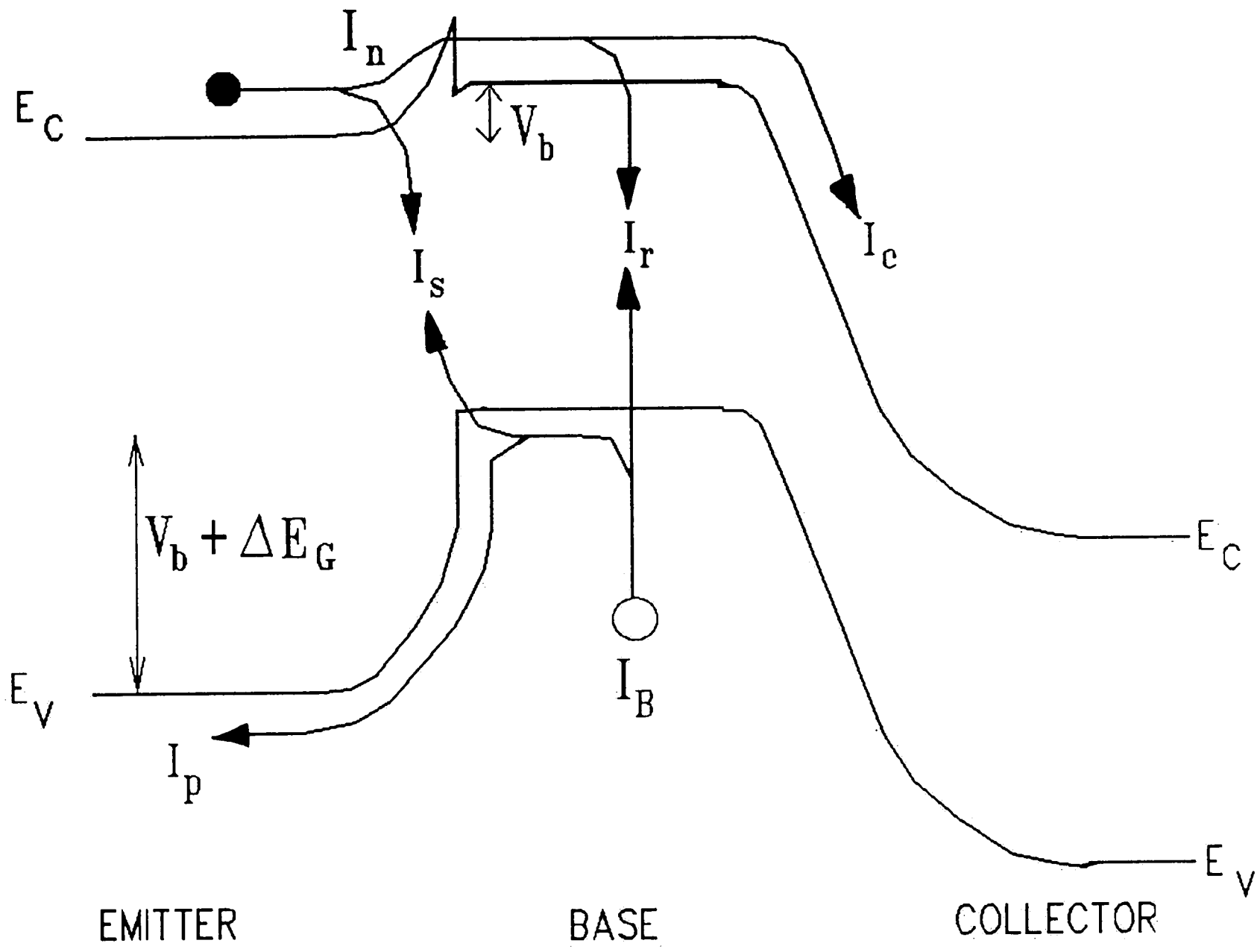

Figure 1. Energy-band diagram of an HBT.

The emitter has a wide bandgap in comparison to the base and collector. This bandgap engineering allows the electrons and holes to be controlled separately, thereby increasing the current injection efficiency across the base-emitter junction.

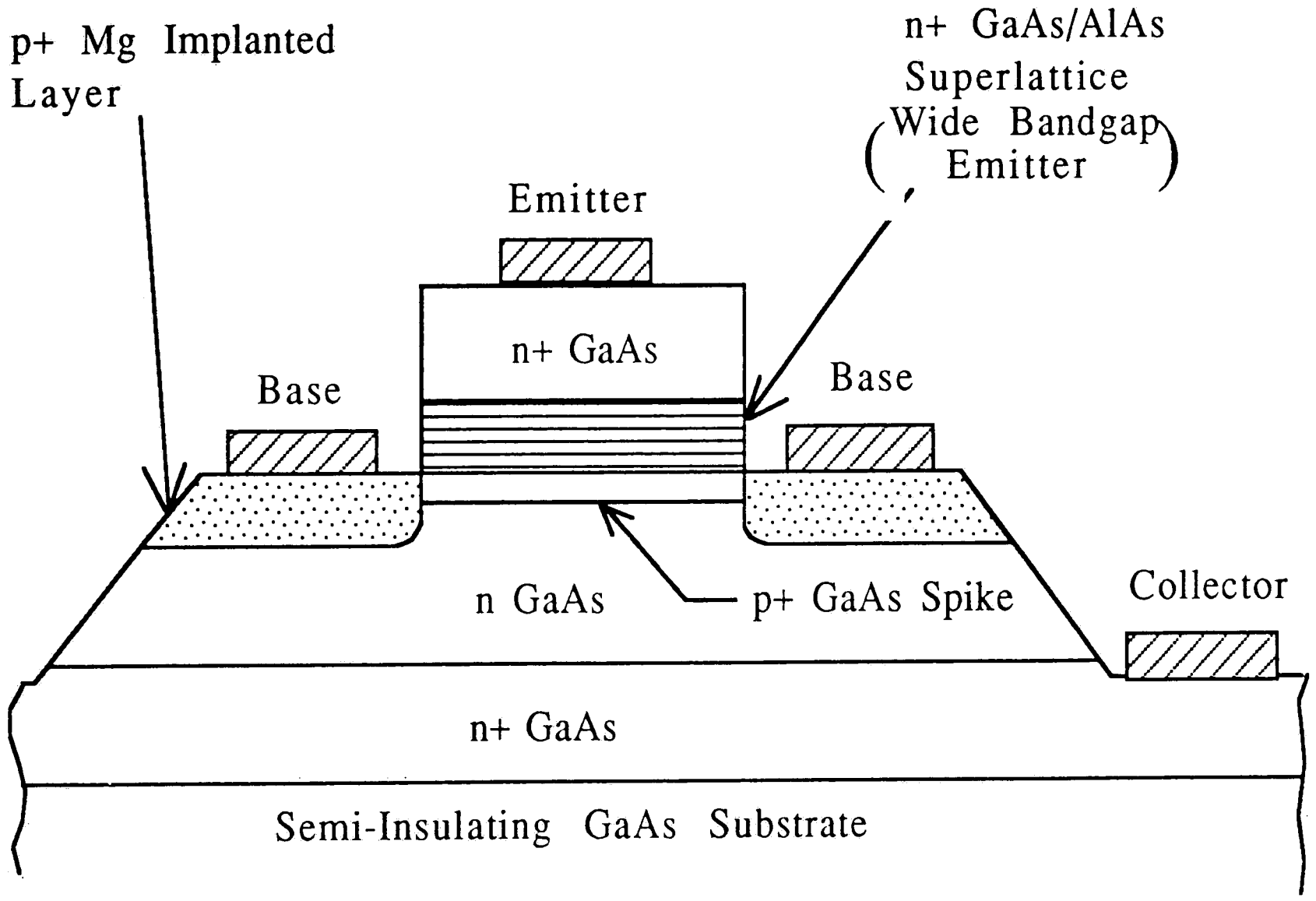

Figure 2. Cross section of an HBT.
Vertical layers are controlled to atomic layer accuracies with epitaxial growth techniques.

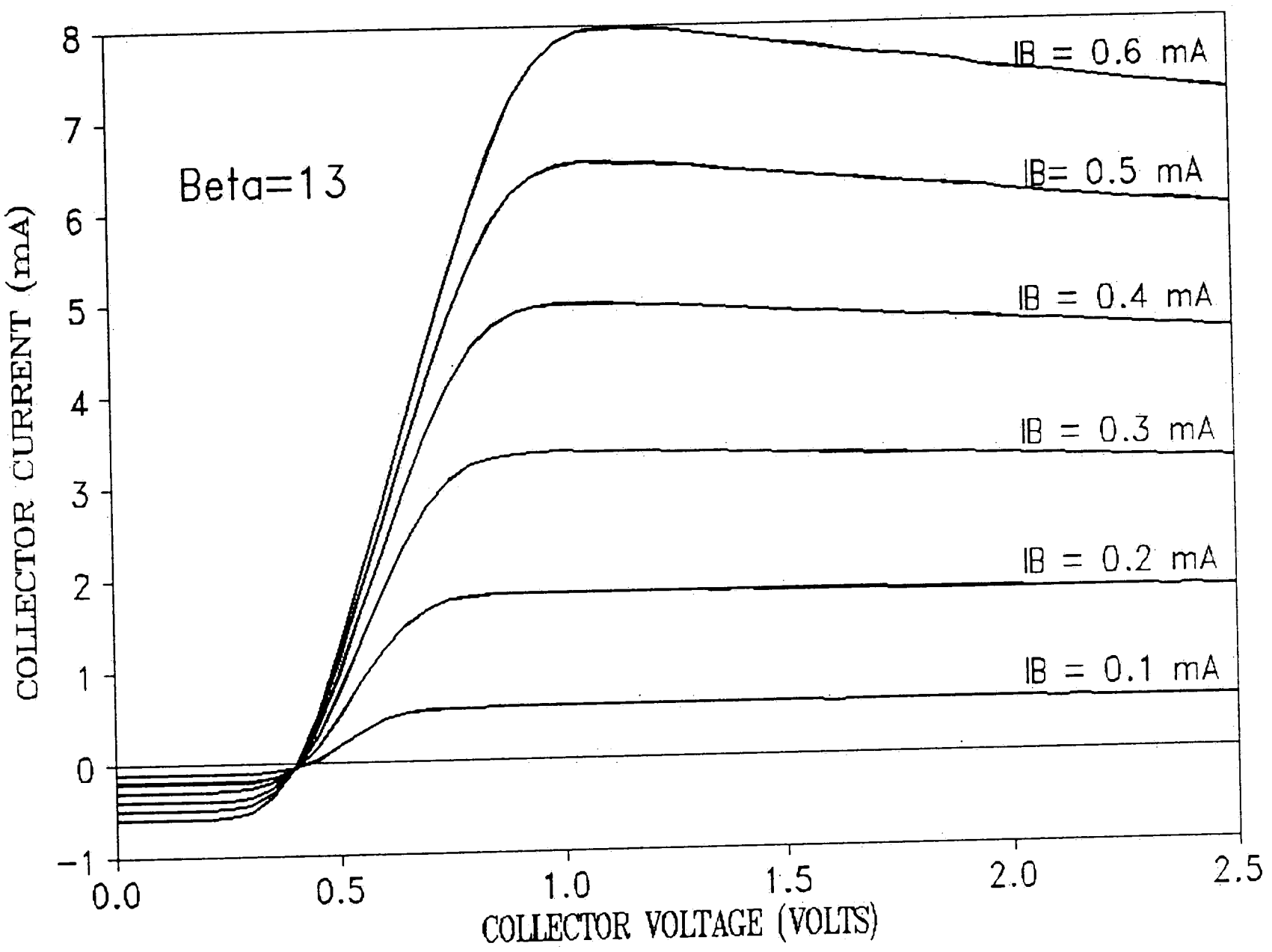

Figure 3. Common emitter I-V characteristics.
HBTs exhibit a finite threshold voltage (0 - 0.4v) due to the nonsymmetric heterojunction. The negative differential resistance at high collector voltages is due to thermal effects.

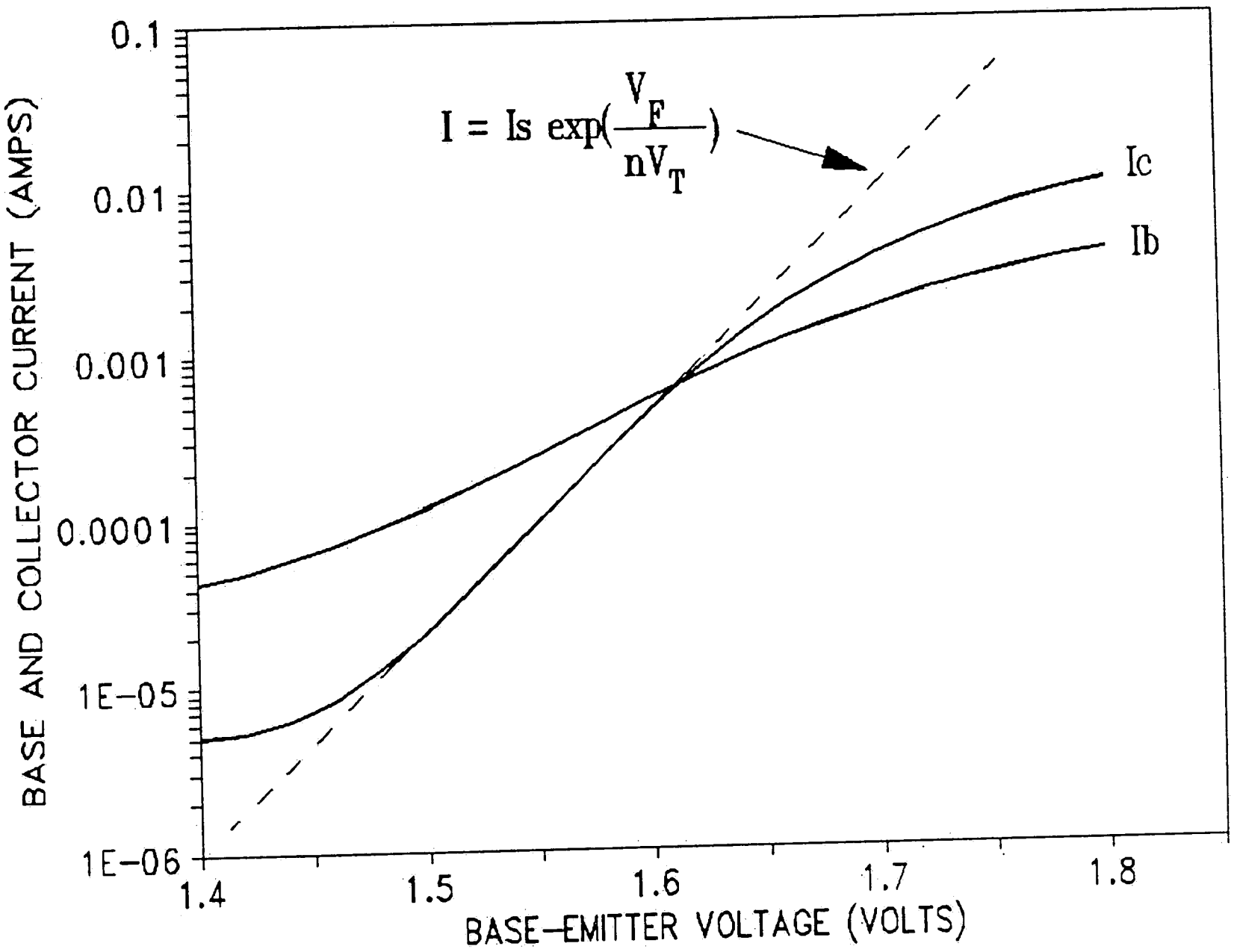

Figure 4. Gummel plot of base and collector currents.
The currents basically follow the diode equation, deviating at low currents due to leakage, and at high currents due to series base and emitter resistance.

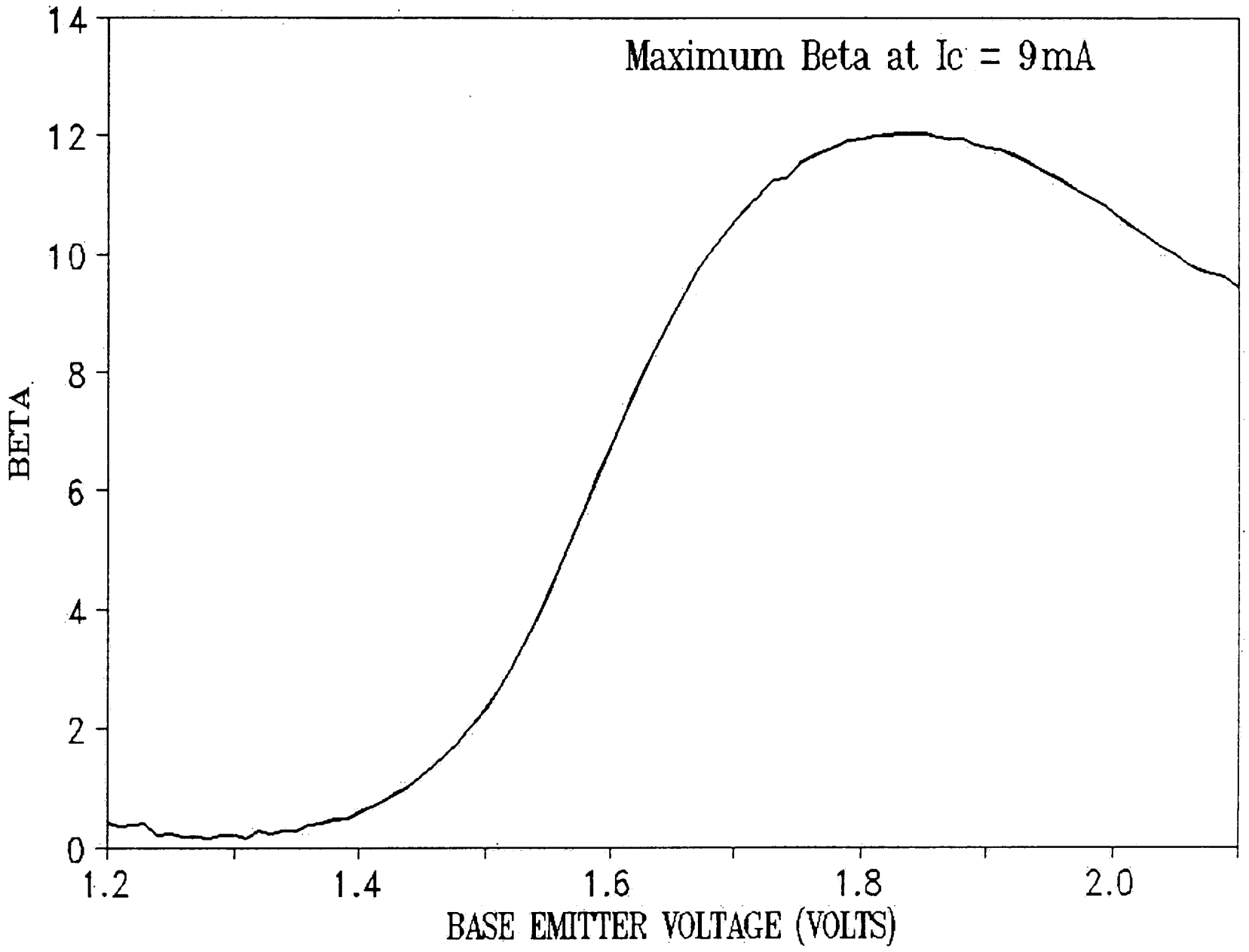

Figure 5. Current gain (β) versus collector current.
The typical reduction of β at low and high current levels is an important factor for large-signal modeling.

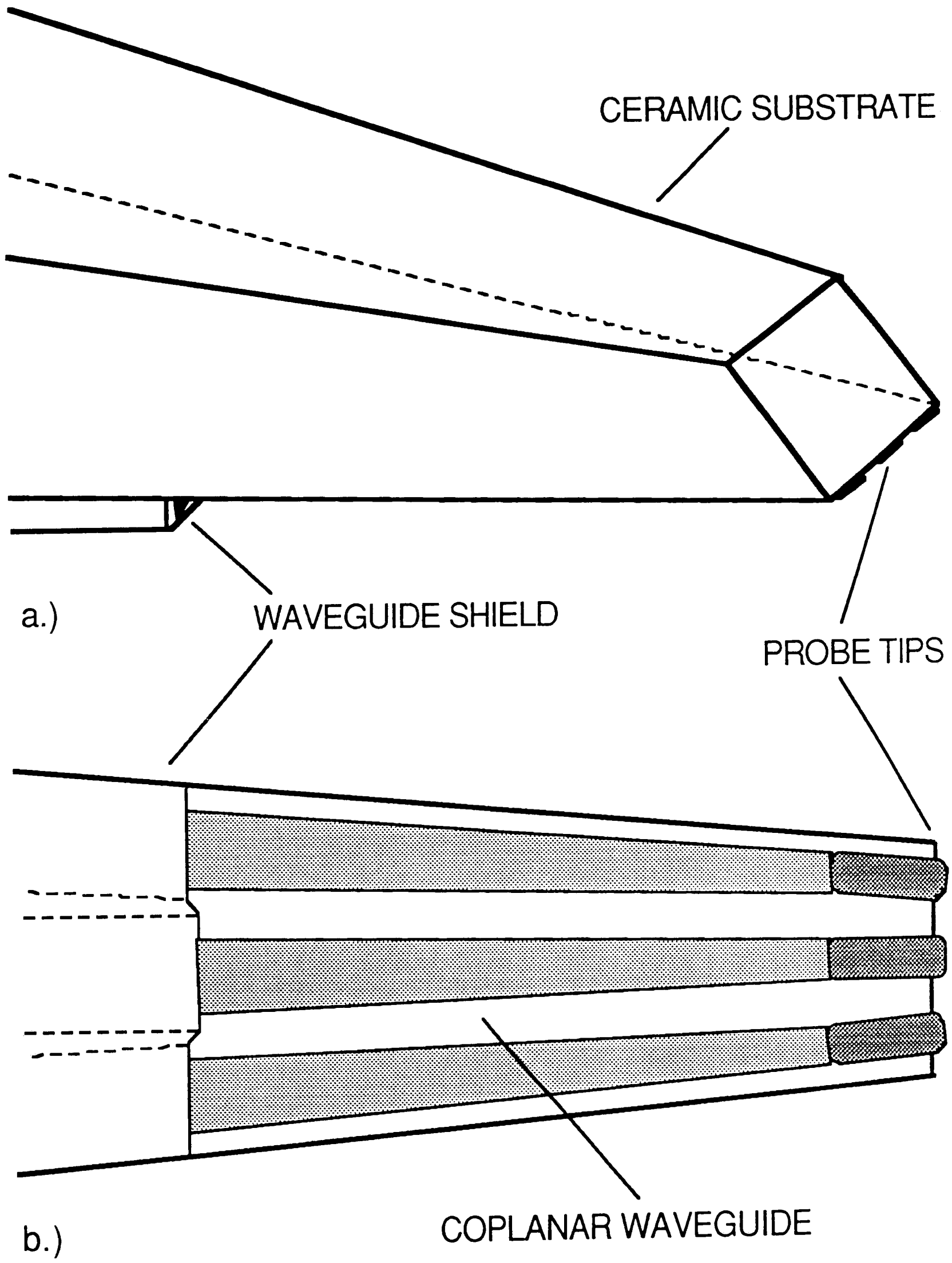

Figure 6. 40GHz Tektronix probes.

a.) Side view with ceramic substrate on top, and metal contact pads on the bottom.
b.) Bottom view of the coplanar waveguide with nickel contact pads at the end.

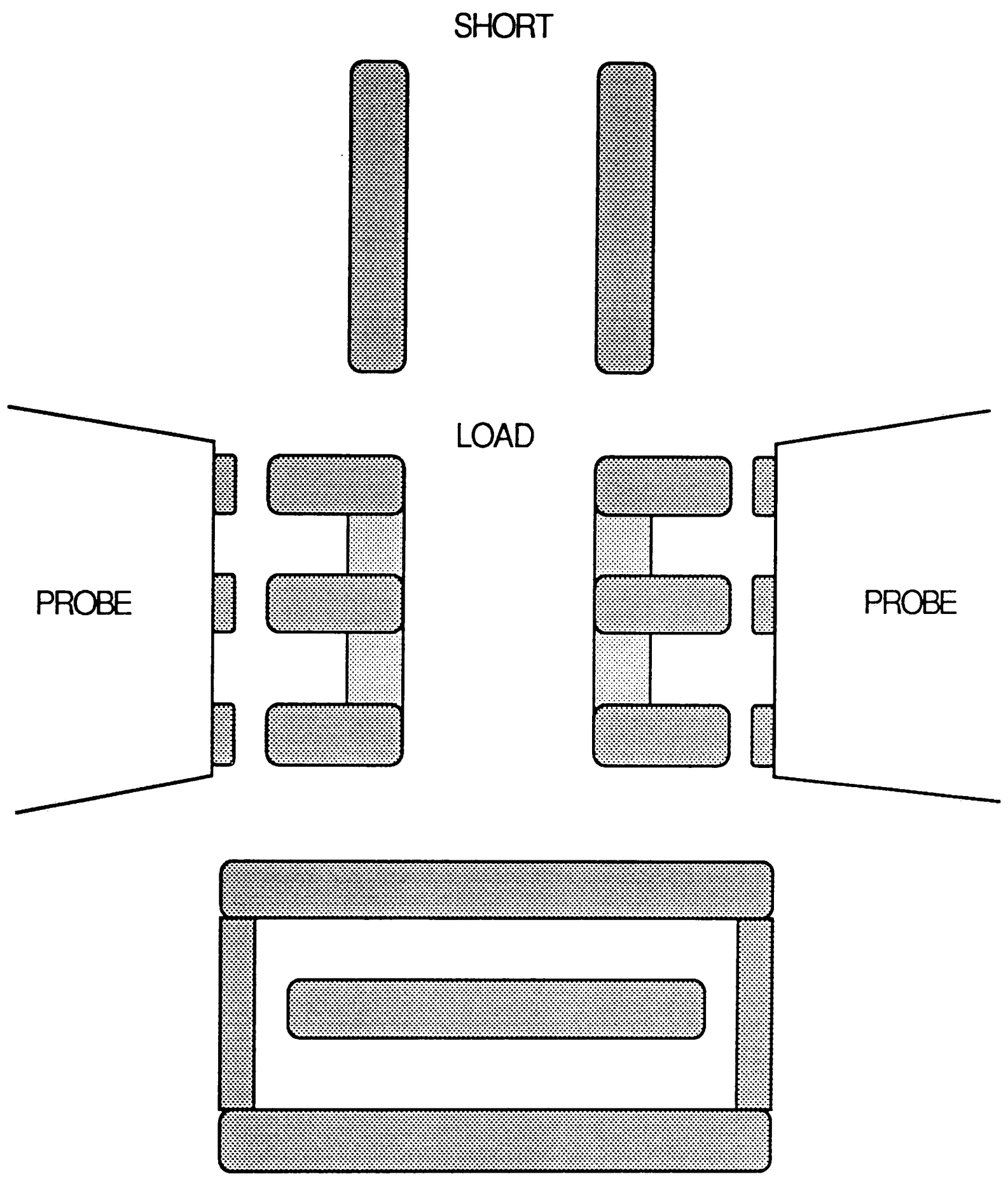

Figure 7. Calibration patterns on the Tektronix wafer.

Short, load, and through patterns are placed on a sapphire substrate for highly accurate on-wafer network analyzer calibrations. RF probes are also shown near the load patterns.

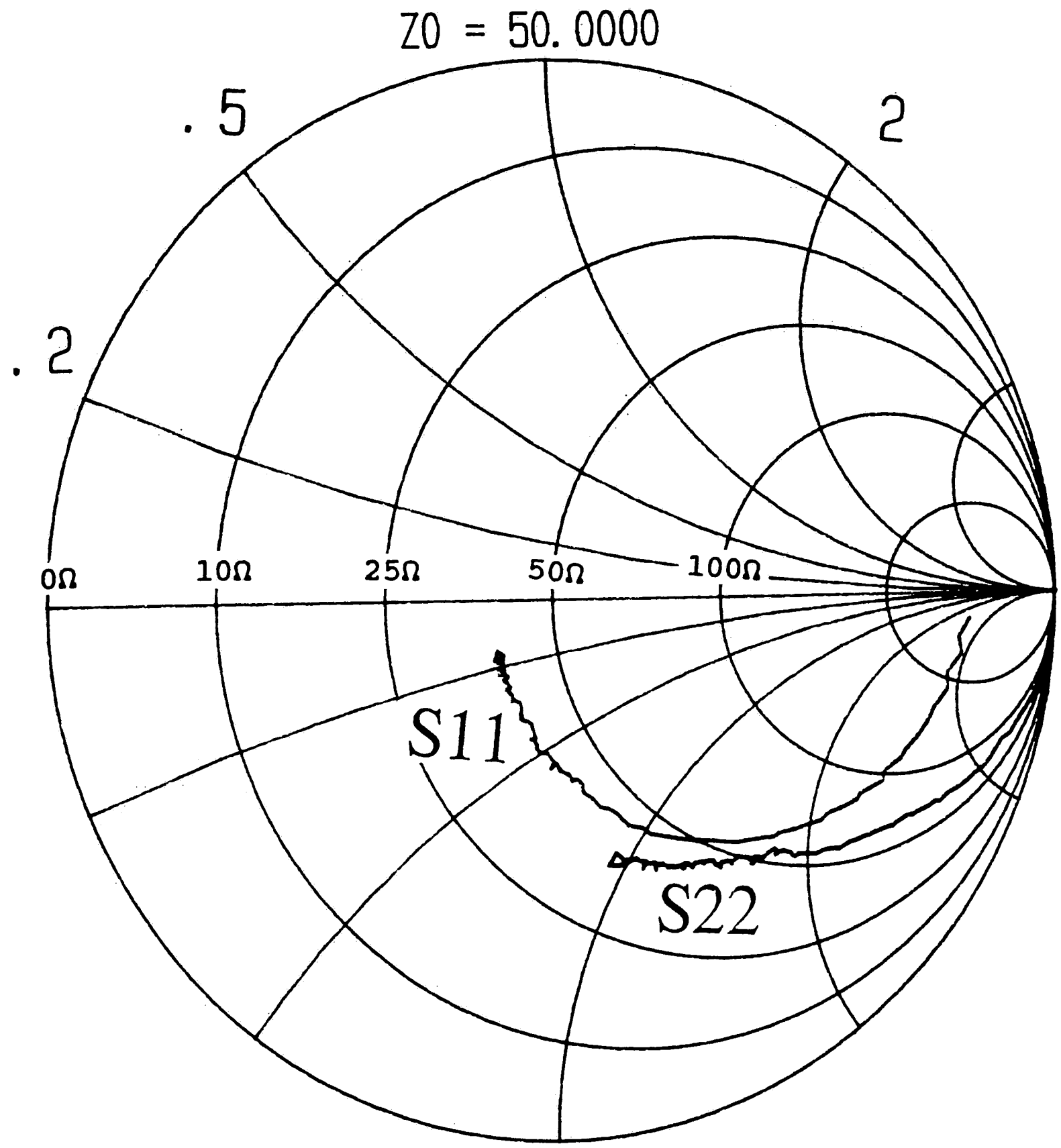

Figure 8. HBT reflection coefficients.

Input reflection (S11) and output reflection (S22) give the input and output complex impedances at microwave frequencies. S11 and S22 are swept from 0.5GHz to 40GHz (right to left).

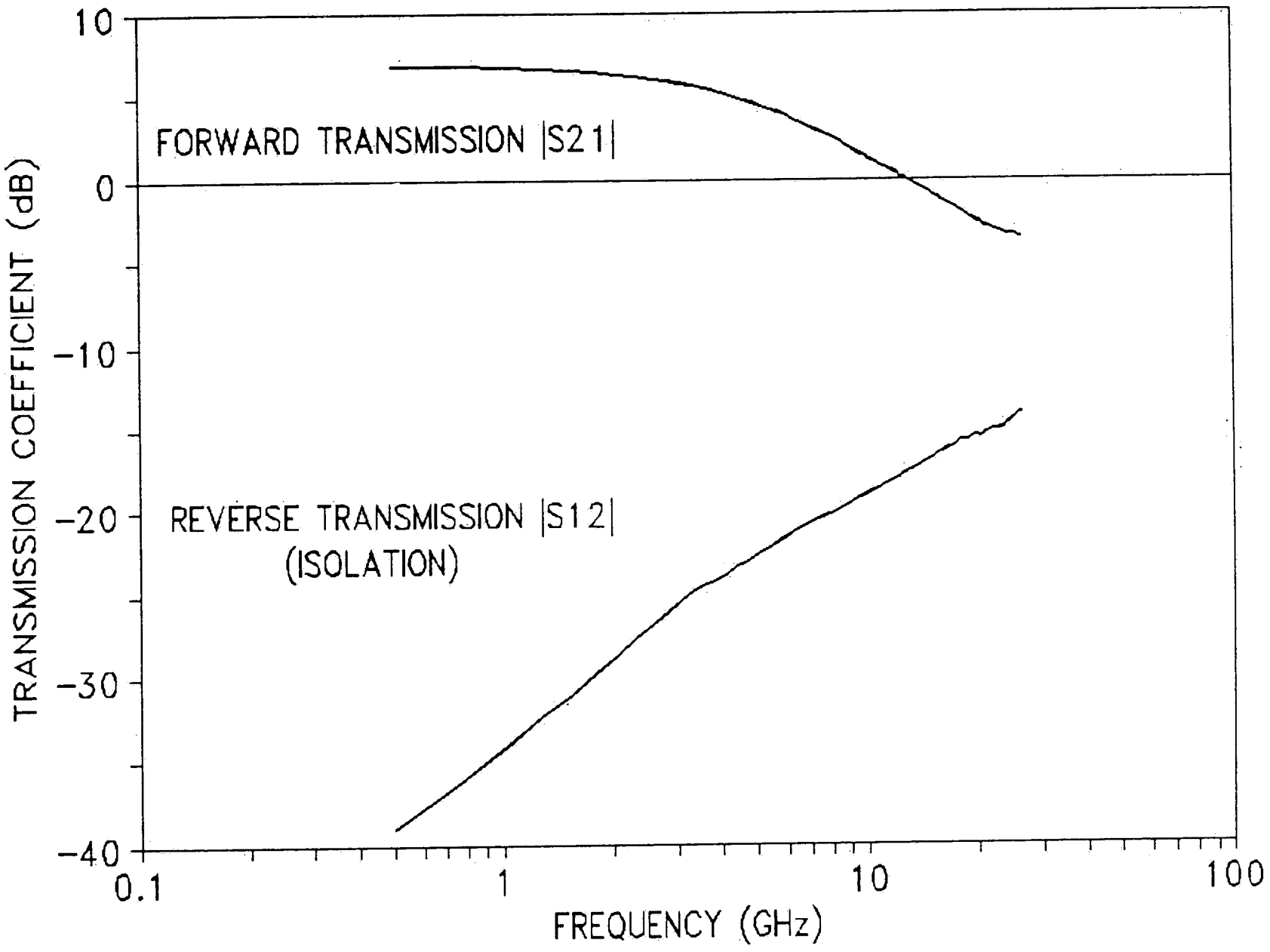

Figure 9. HBT transmission coefficients.
Forward transmission (S21) and reverse transmission (S12), show forward gain and good reverse isolation.

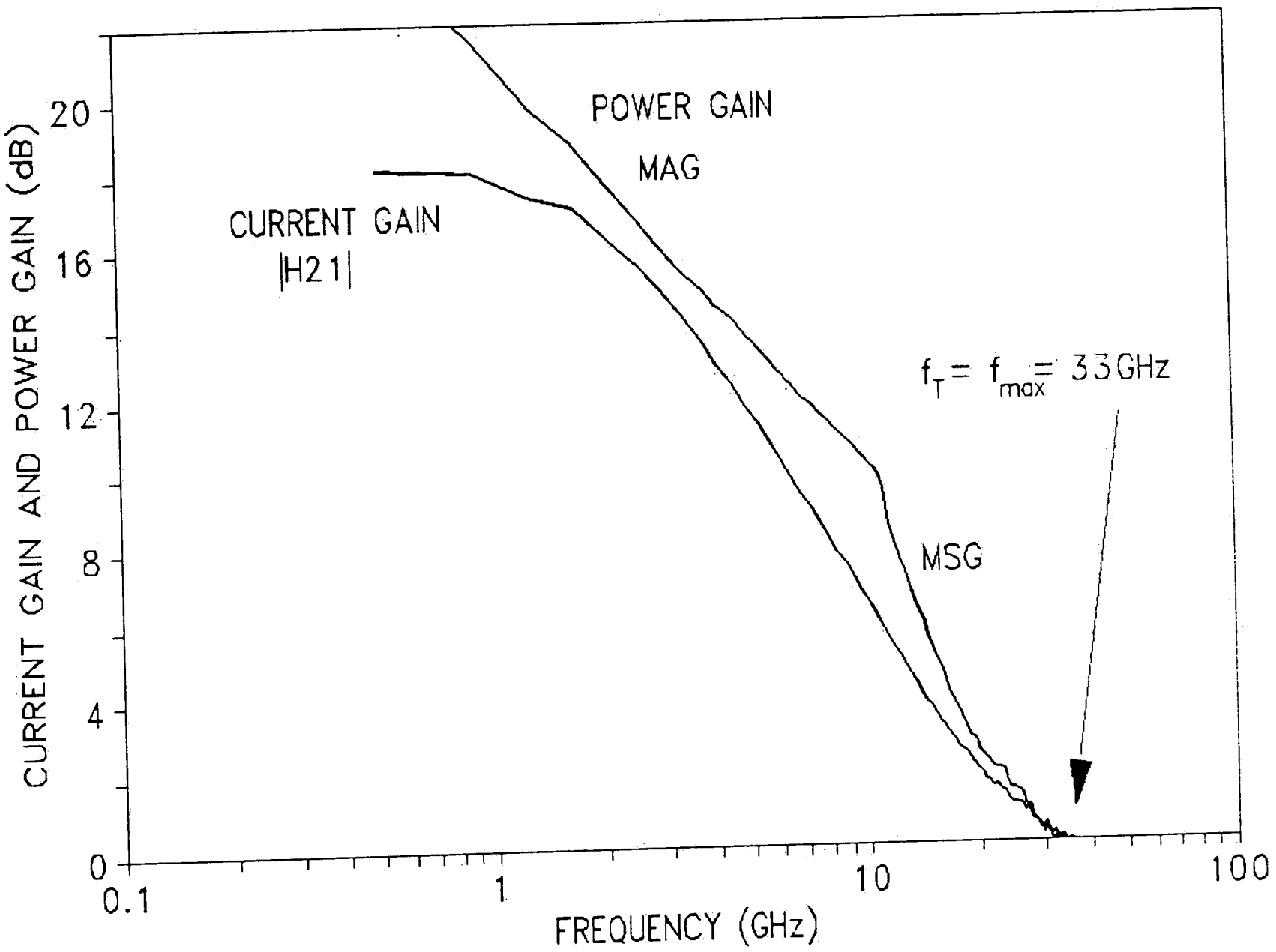

Figure 10. Forward current gain and power gain.
Forward current gain ($|H21|$) has a unity gain at $f_T = 33GHz$. Power Gain (MSG and MAG) has a cutoff at $f_{max} = 33GHz$ also.

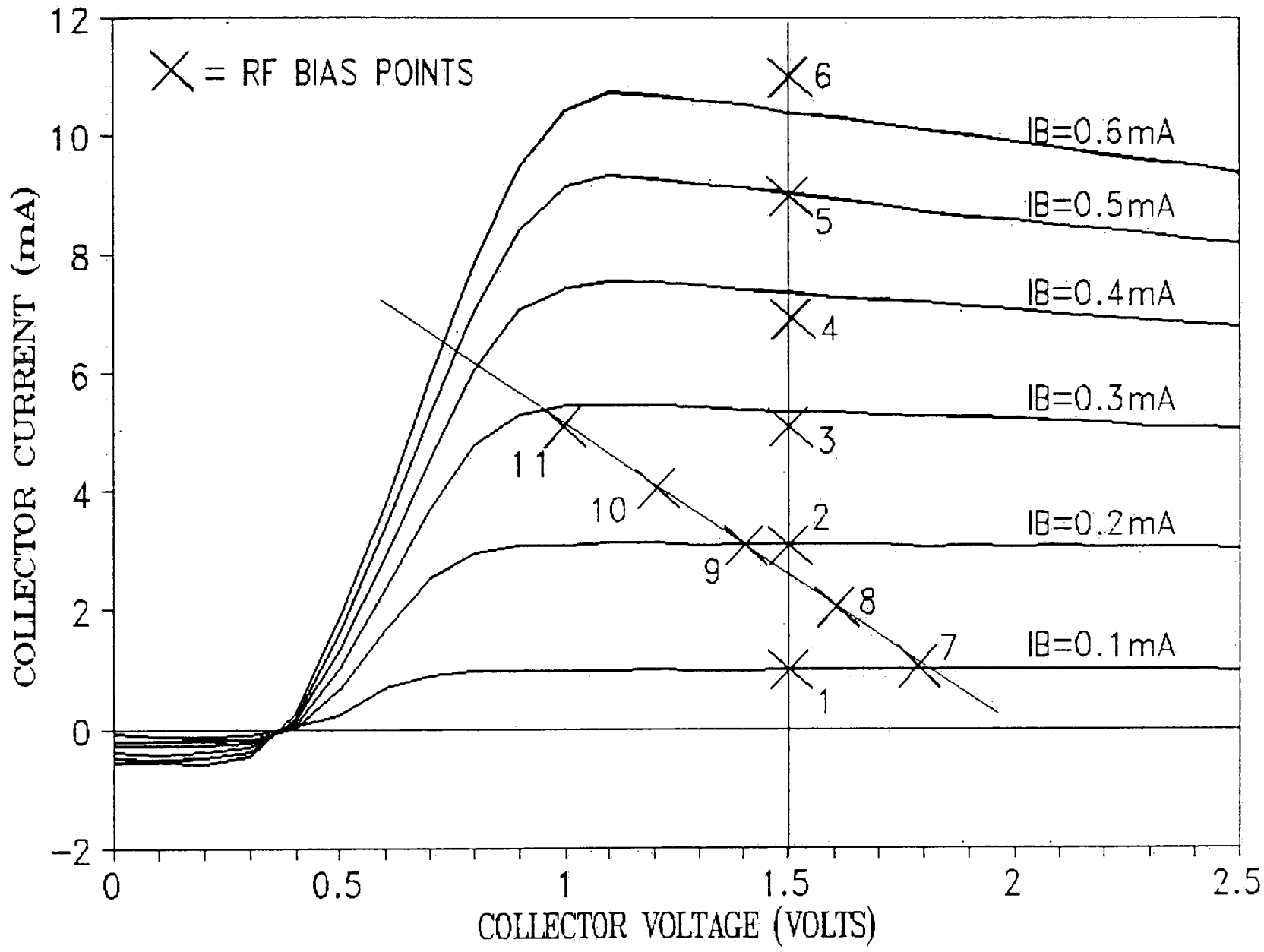

Figure 11. Bias points for RF measurements.

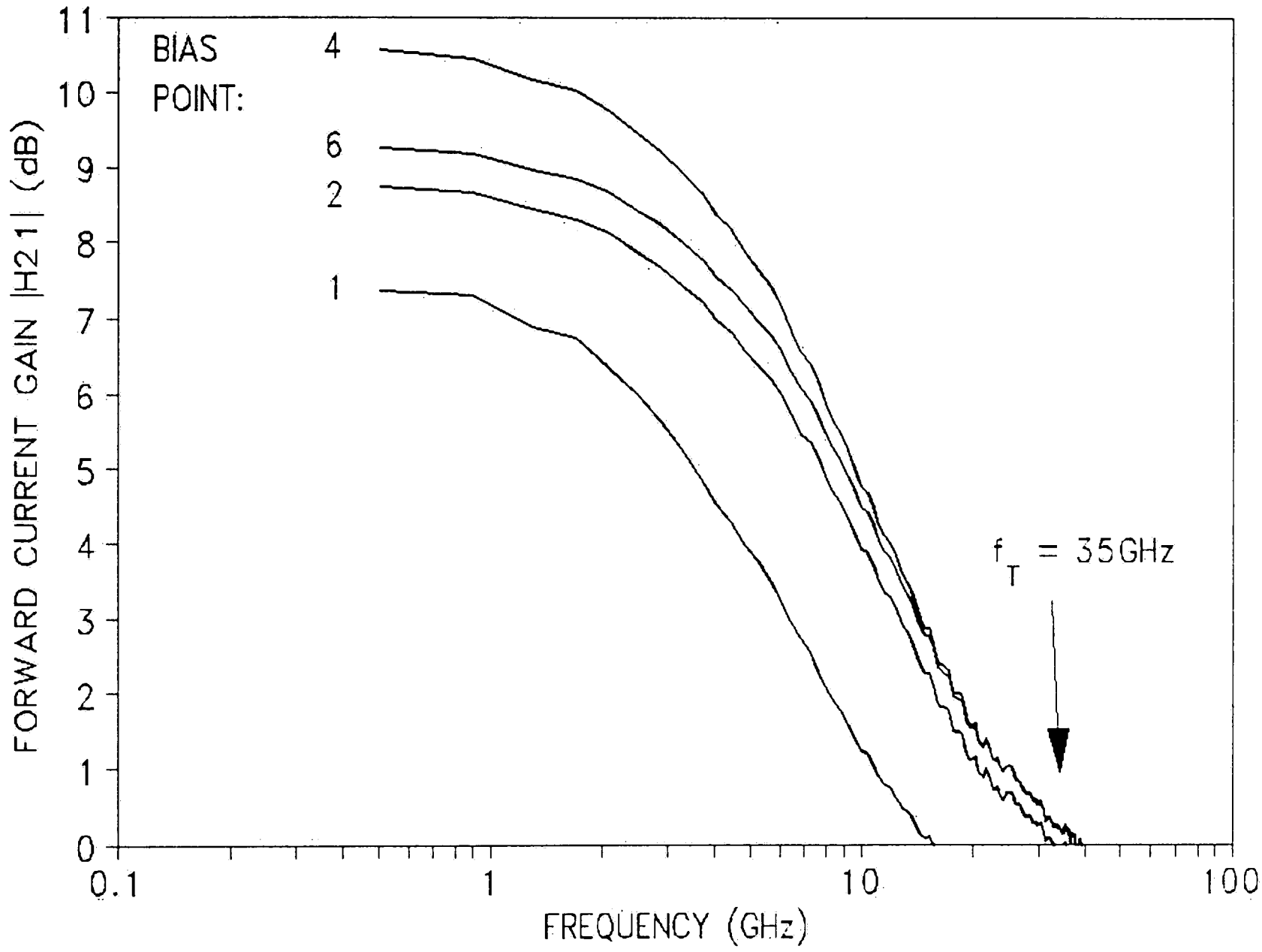

Figure 12. RF current gain for various bias points.

Current gain drops at low and high currents as in DC measurements.

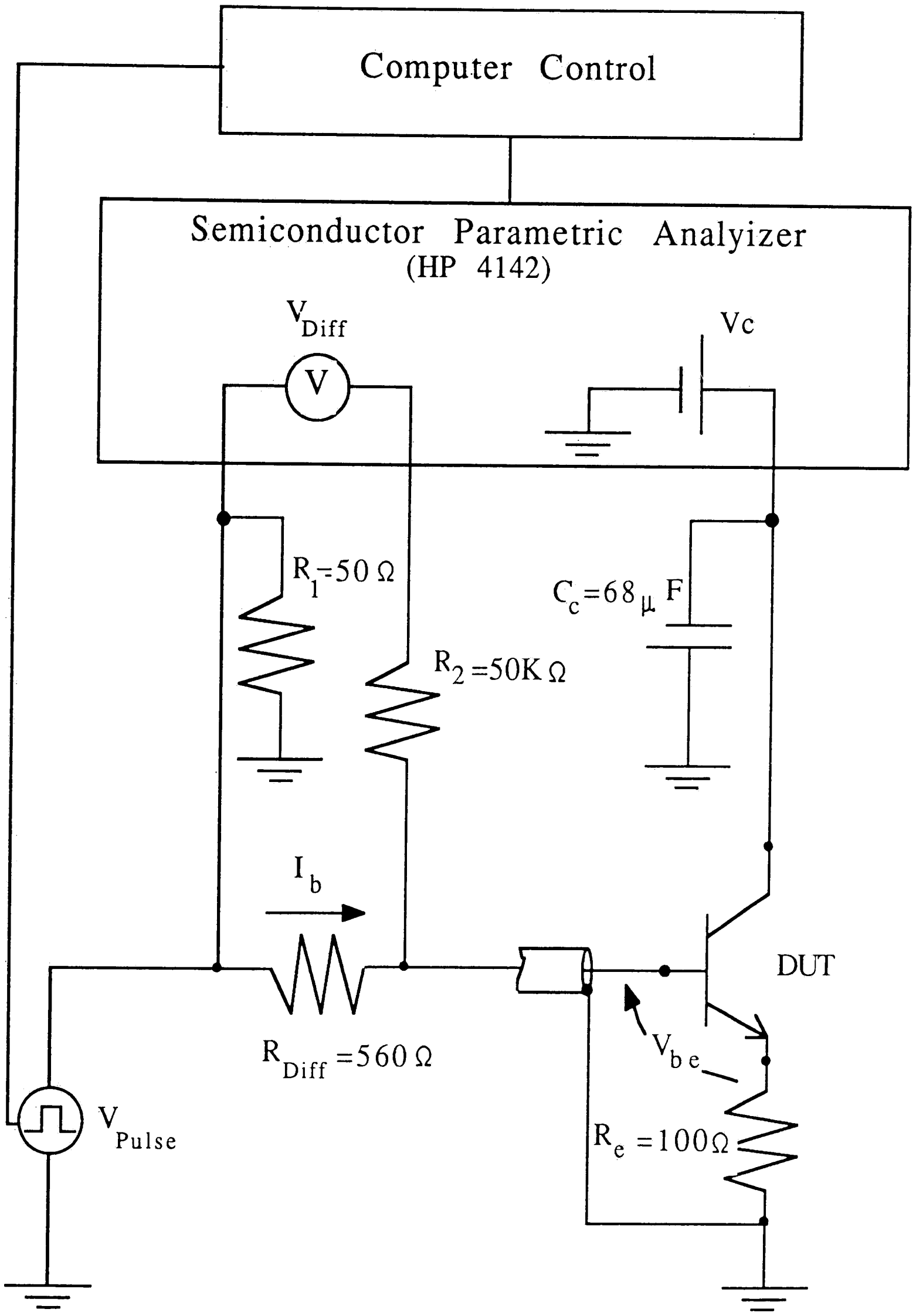

Figure 13. Pulsed measurement setup.

Pulses of constant current are applied to the base of the HBT and the average collector current is measured. The actual pulsed collector current value is calculated from the known duty cycle.

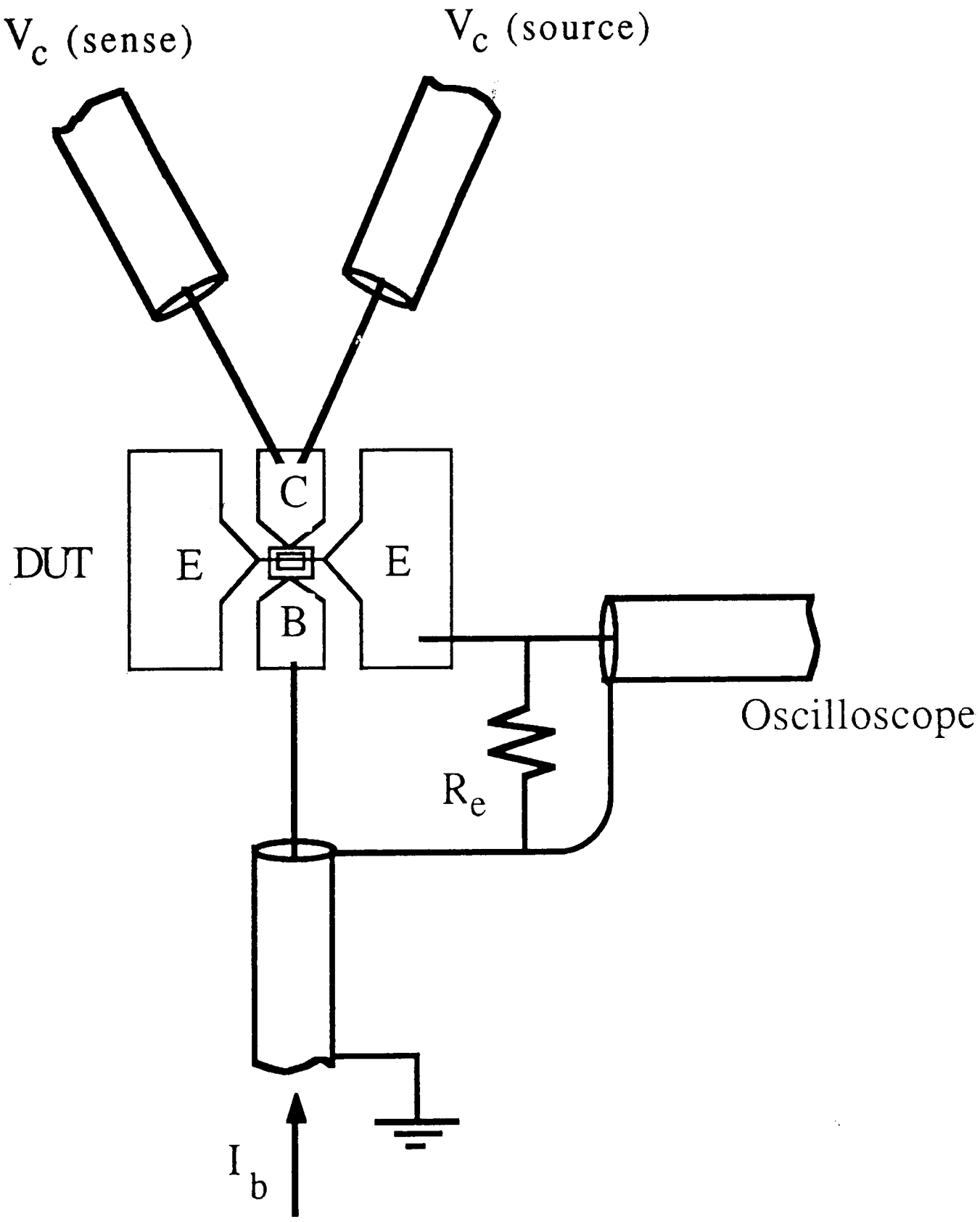

Figure 14. Probe positioning for pulsed setup.

Local grounding between the base and emitter was found to be important. R_e is included to monitor the emitter current with an oscilloscope.

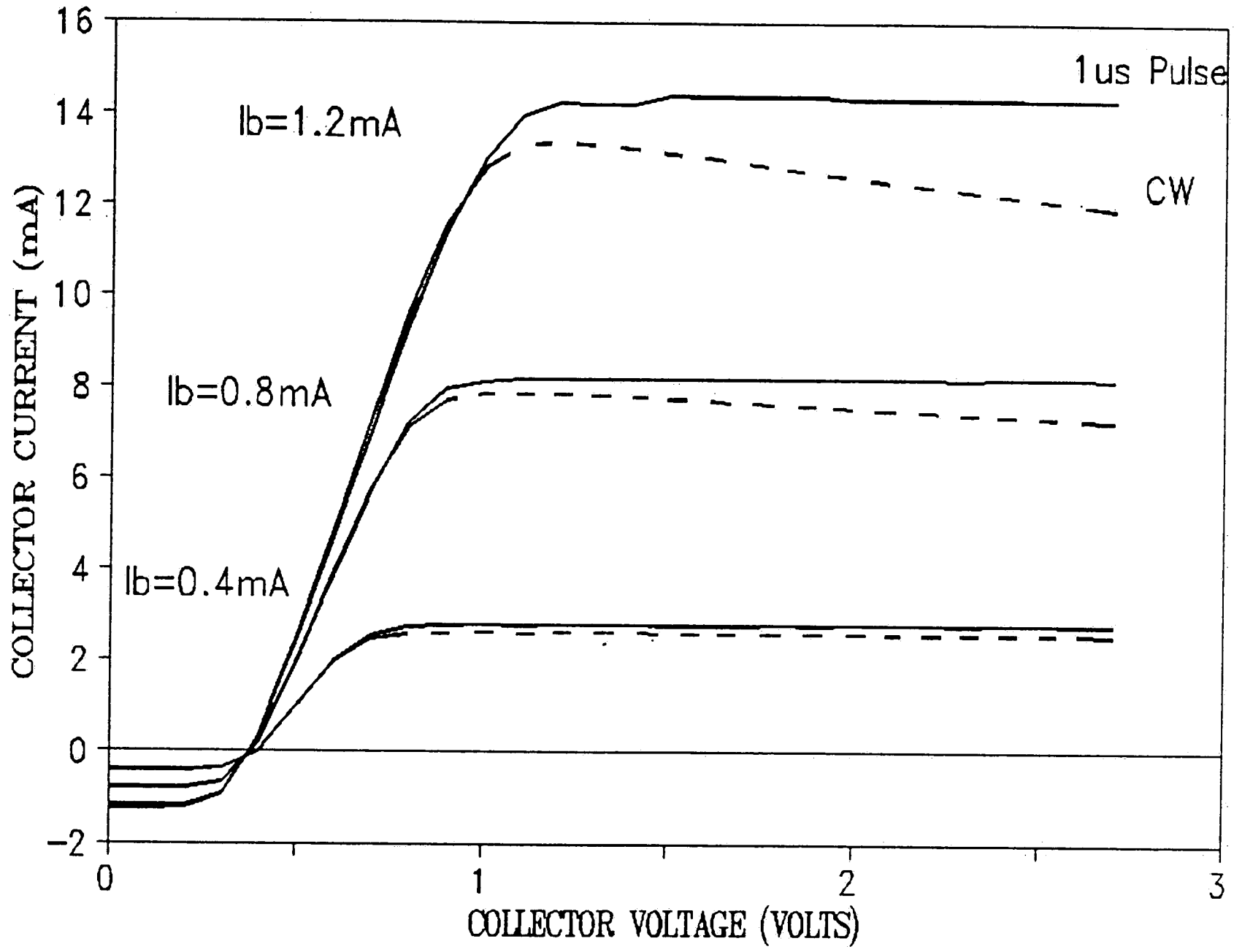

Figure 15. Pulsed I-V characteristics.
Thermal effects are significantly reduced with a 1μs pulsed base current.

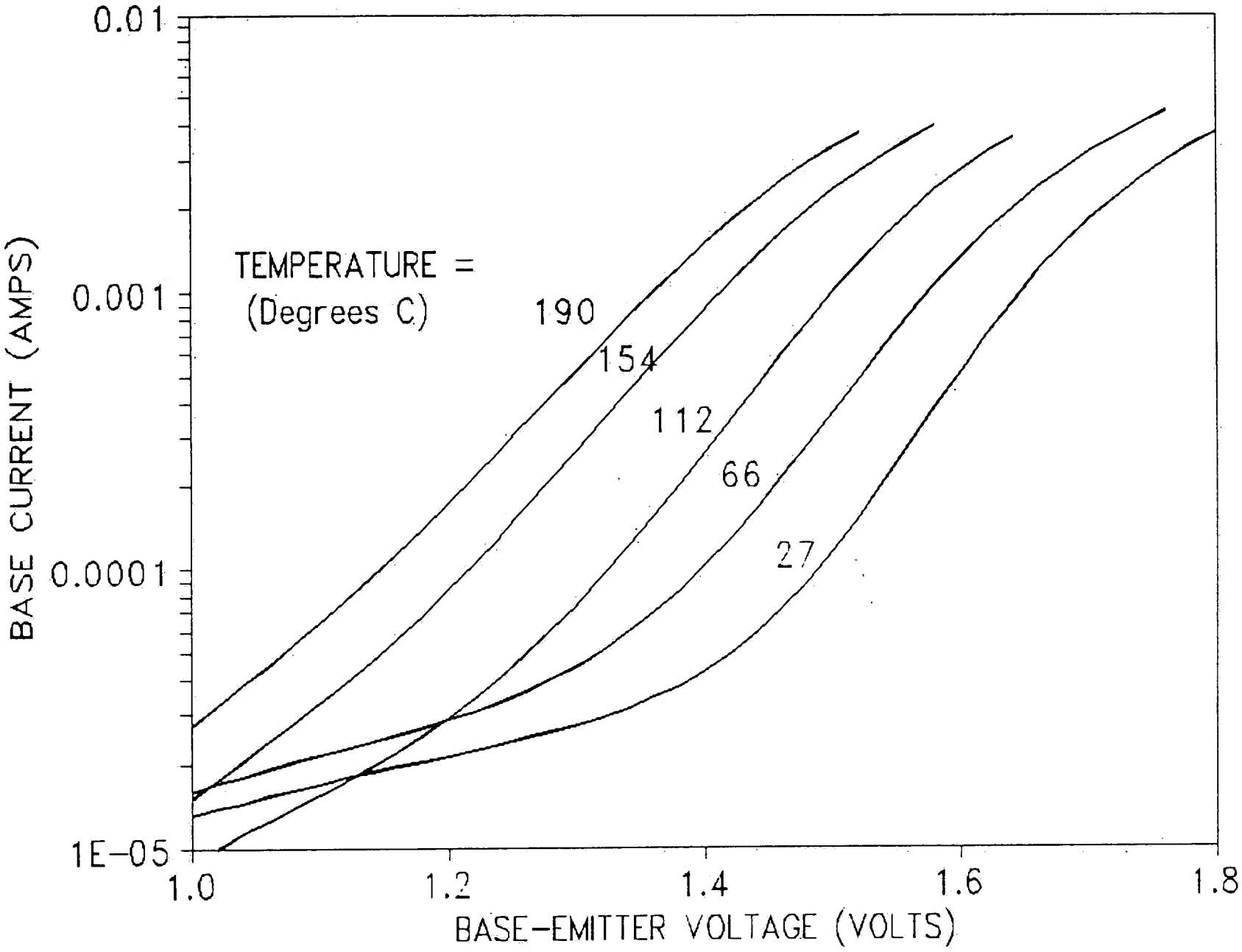

Figure 16. Dependence of base current on V_{be} and temperature.
The base current has a strong and predictable dependence on temperature.

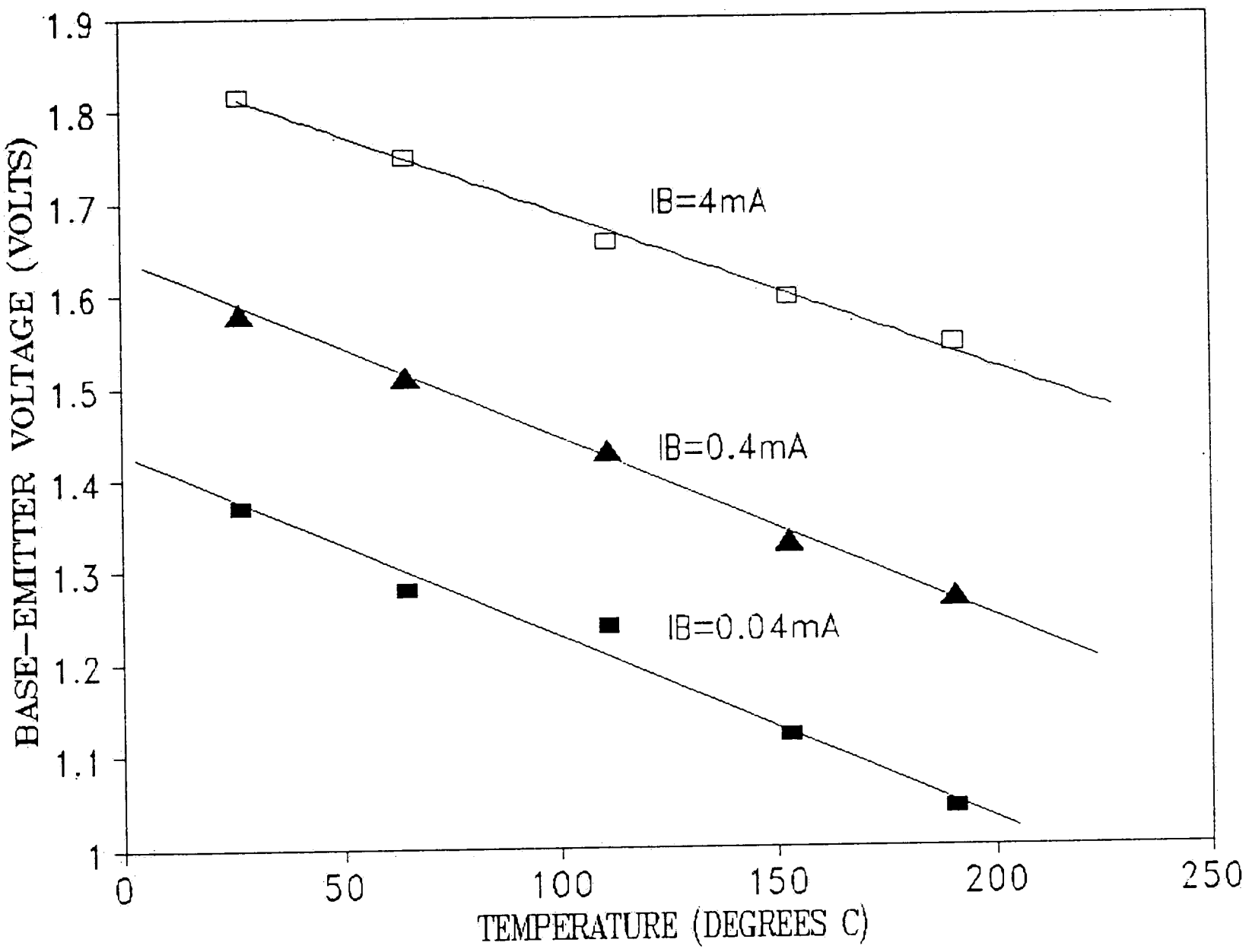

Figure 17. Temperature dependence of base-emitter voltage.

For a constant base current, V_{be} has essentially a linear dependence on temperature. For low current levels ($I_b < 1e^{4}$ A/cm^2), this follows the theoretical behavior well.

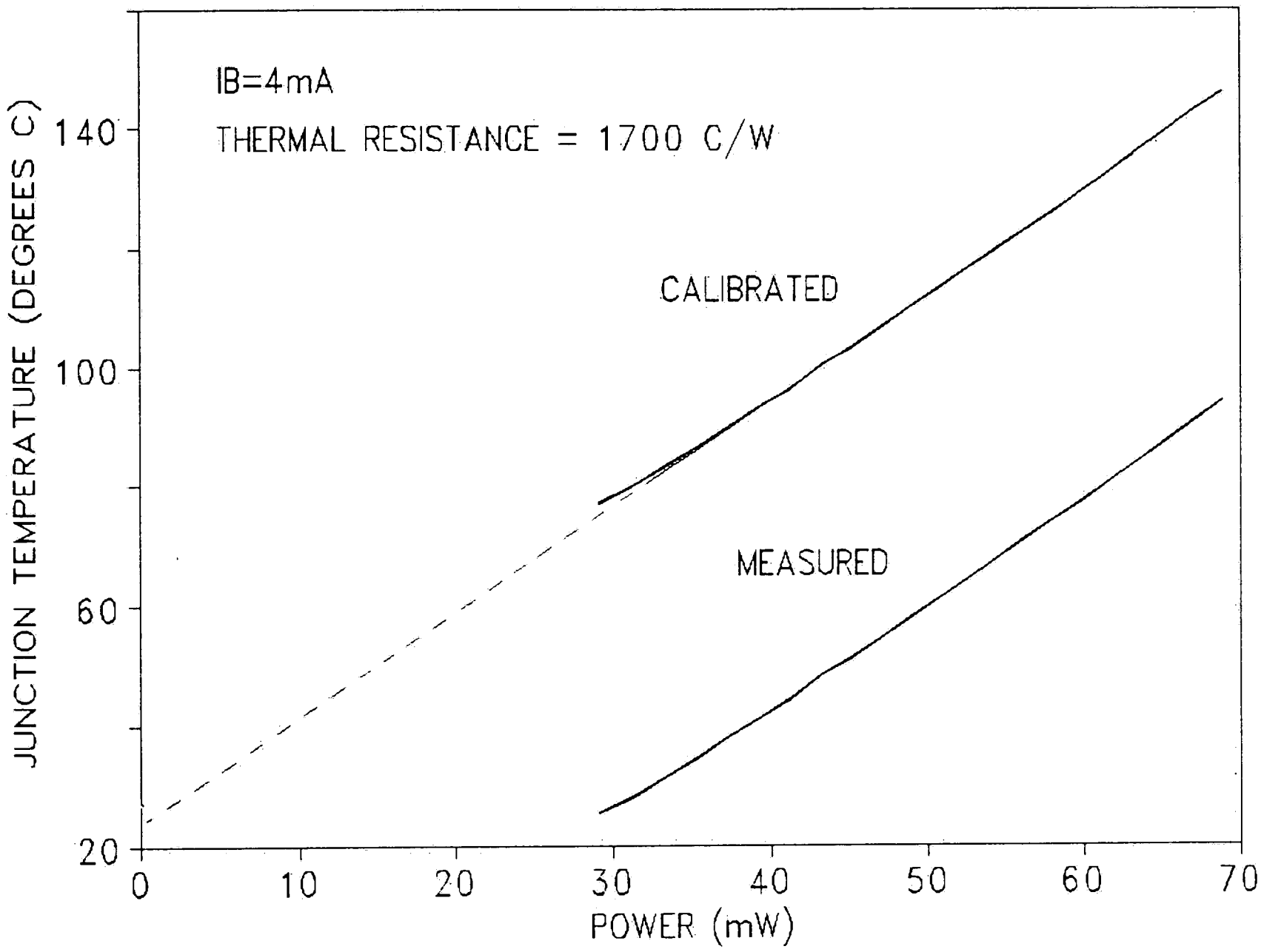

Figure 18. Measured and calibrated HBT junction temperature.

The junction temperature is deduced from the dependence of V_{be} on temperature. Due to finite power dissipation in the transistor the correct junction temperature must be calibrated to predict room temperature at zero power.

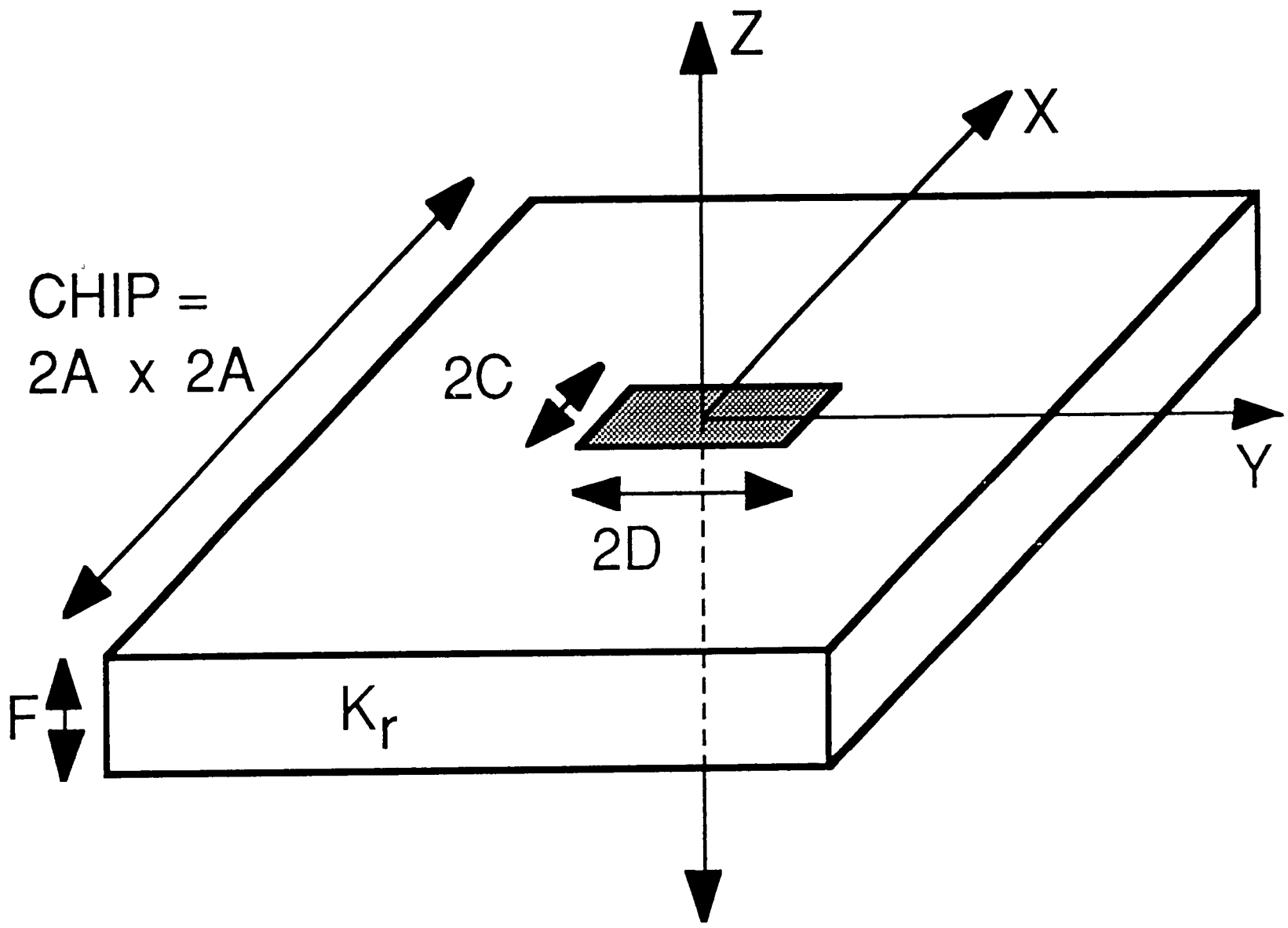

Figure 19. Chip geometry for heat flow analysis.

A semiconductor chip of dimensions 2A x 2A x F is the geometry used to calculate the thermal resistance from a 2C x 2D emitter to a constant temperature bottom plate. All other surfaces are assumed to be adiabatic.

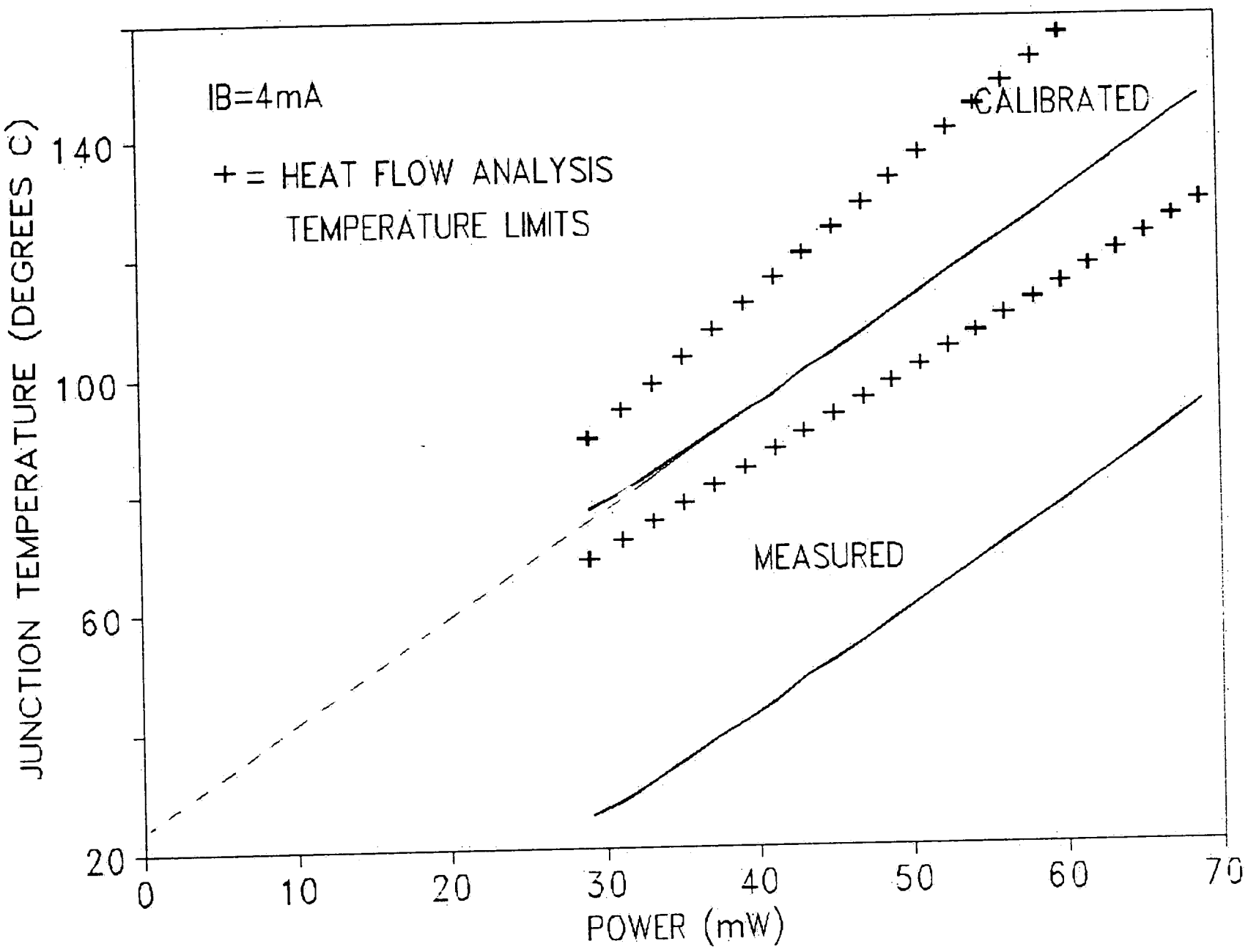

Figure 20. Junction temperature comparison to chip model.

The calibrated junction temperature falls within the maximum and minimum temperatures as computed from the chip dimensions.

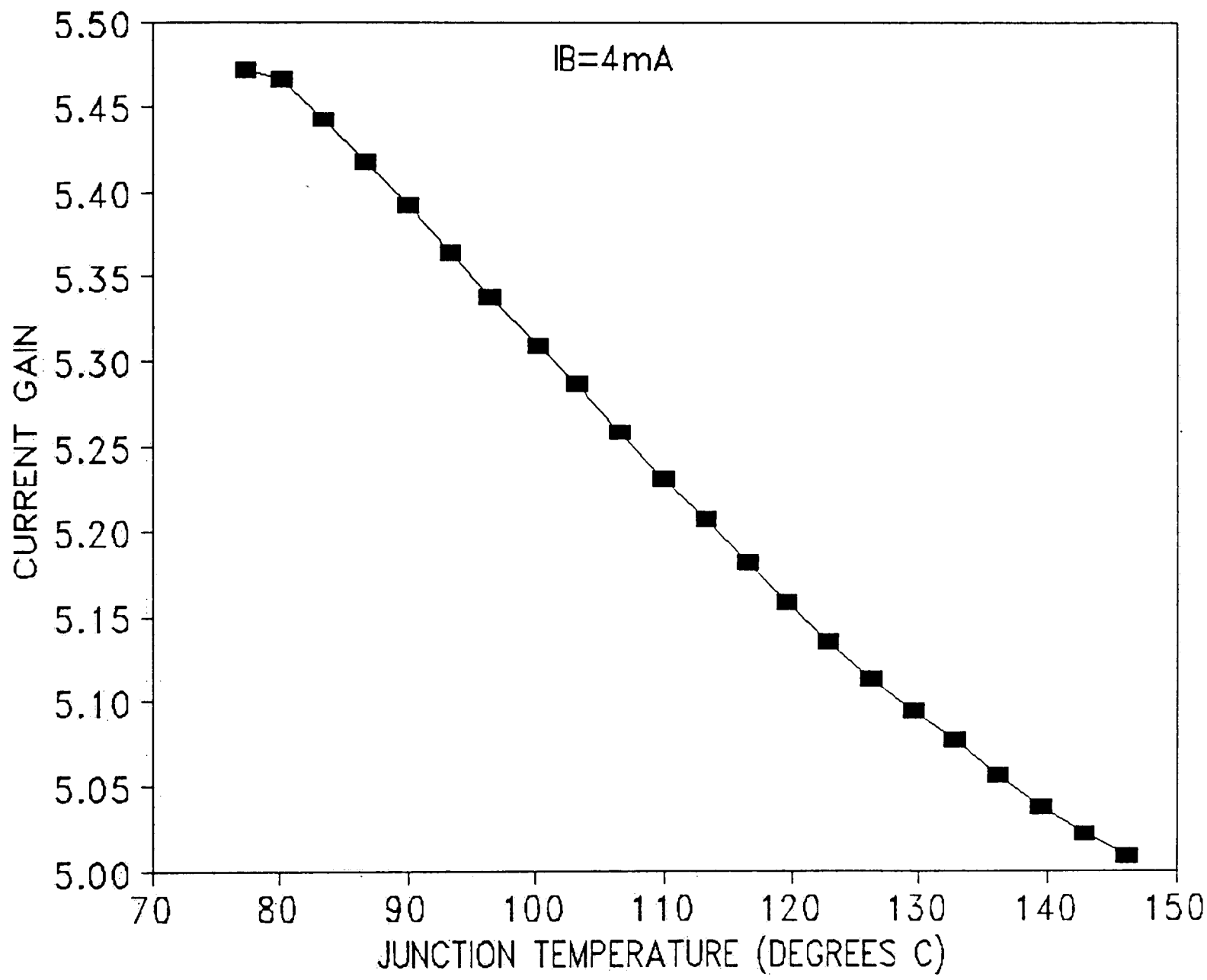

Figure 21. Current gain versus temperature.
The current gain reduction is almost linear with temperature.

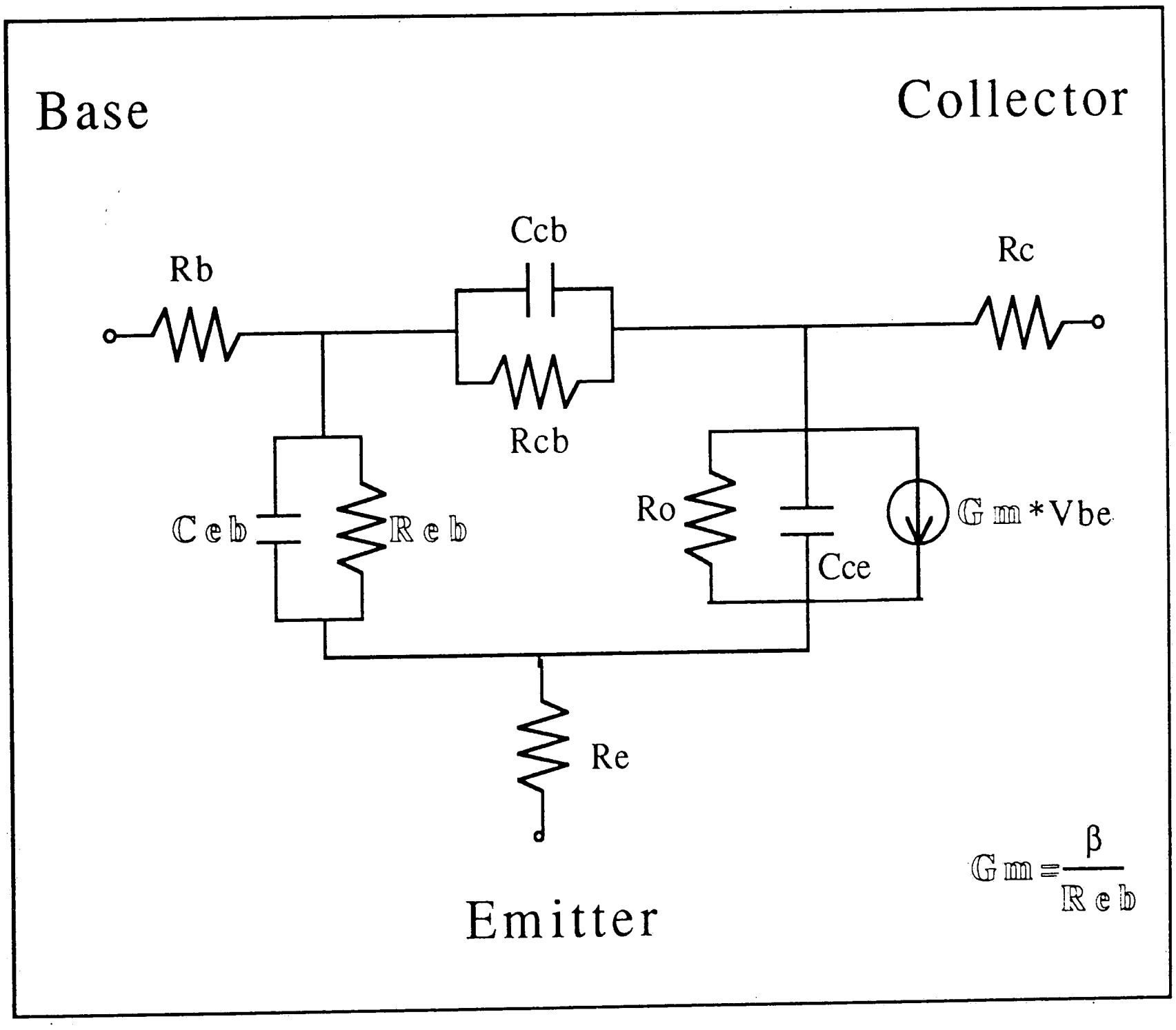

Figure 22. Bias dependent equivalent circuit model.

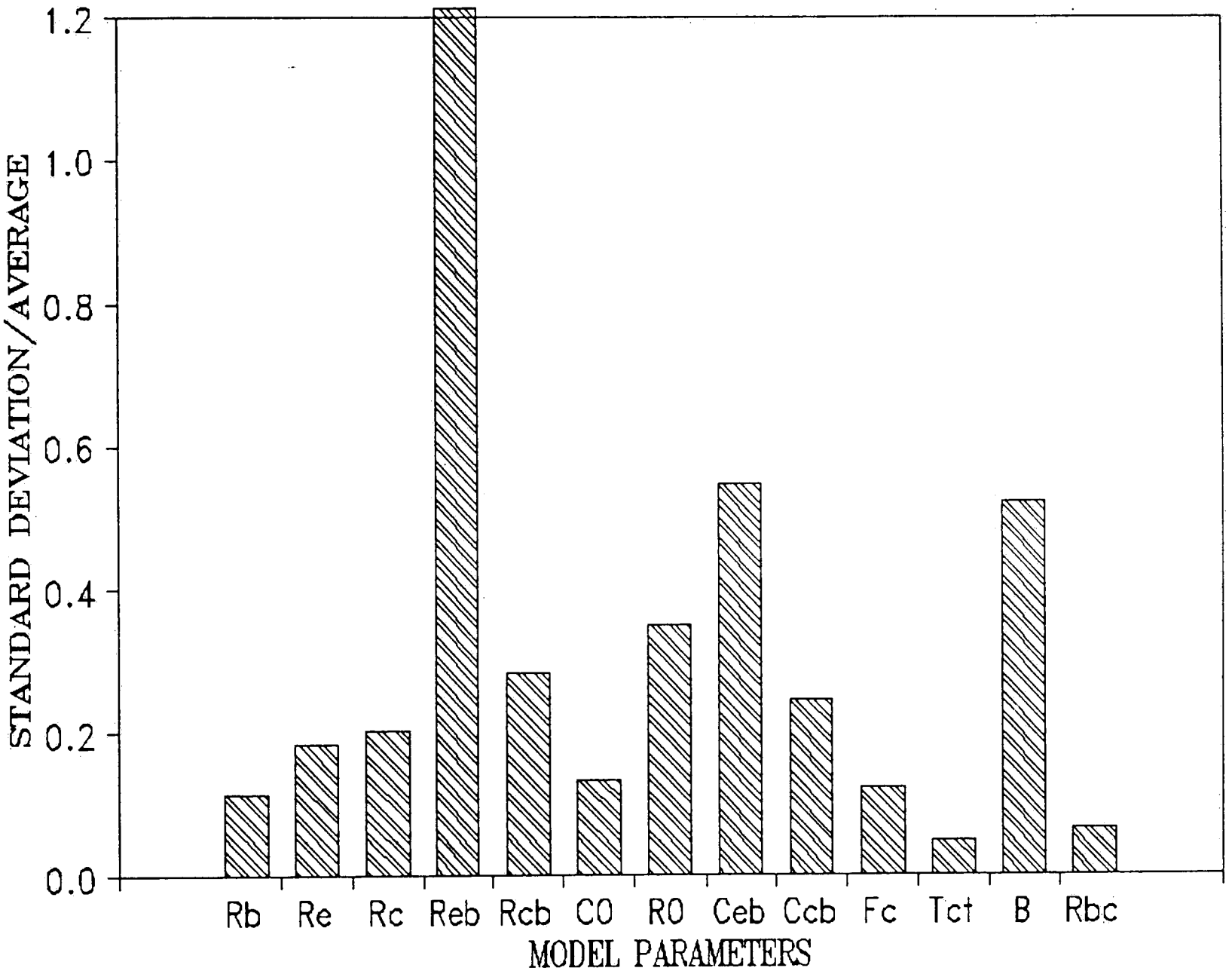

Figure 23. Variation of model parameters with bias.
Ceb, Reb, and β are seen to vary the greatest with bias. All others will be held constant in the final analysis.

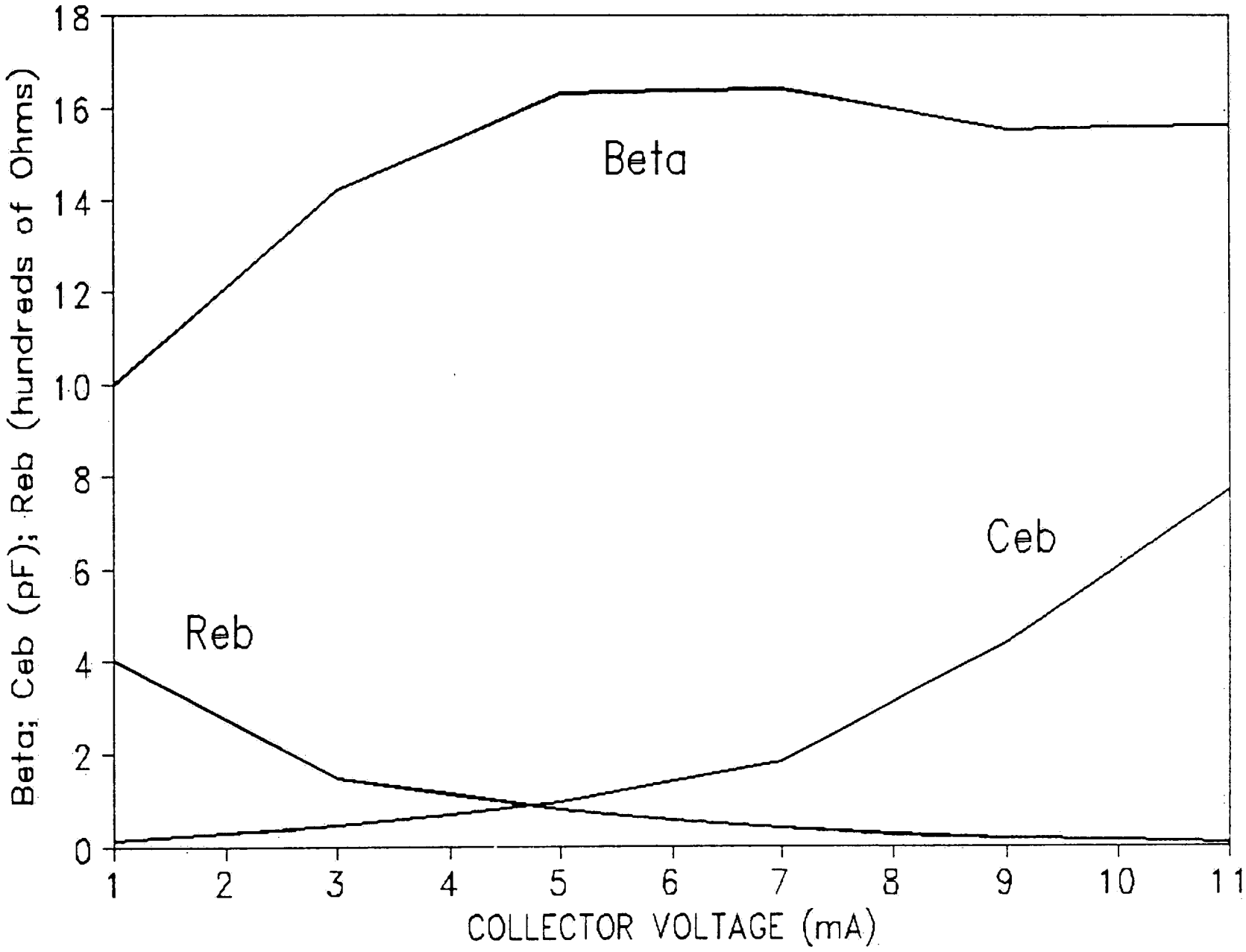

Figure 24. Bias dependence of key nonlinear elements.

All three elements which are allowed to vary with bias show non-linear dependence on the collector current. Reb and Ceb are essentially exponential functions, while β shows the typical reduction at high and low currents.

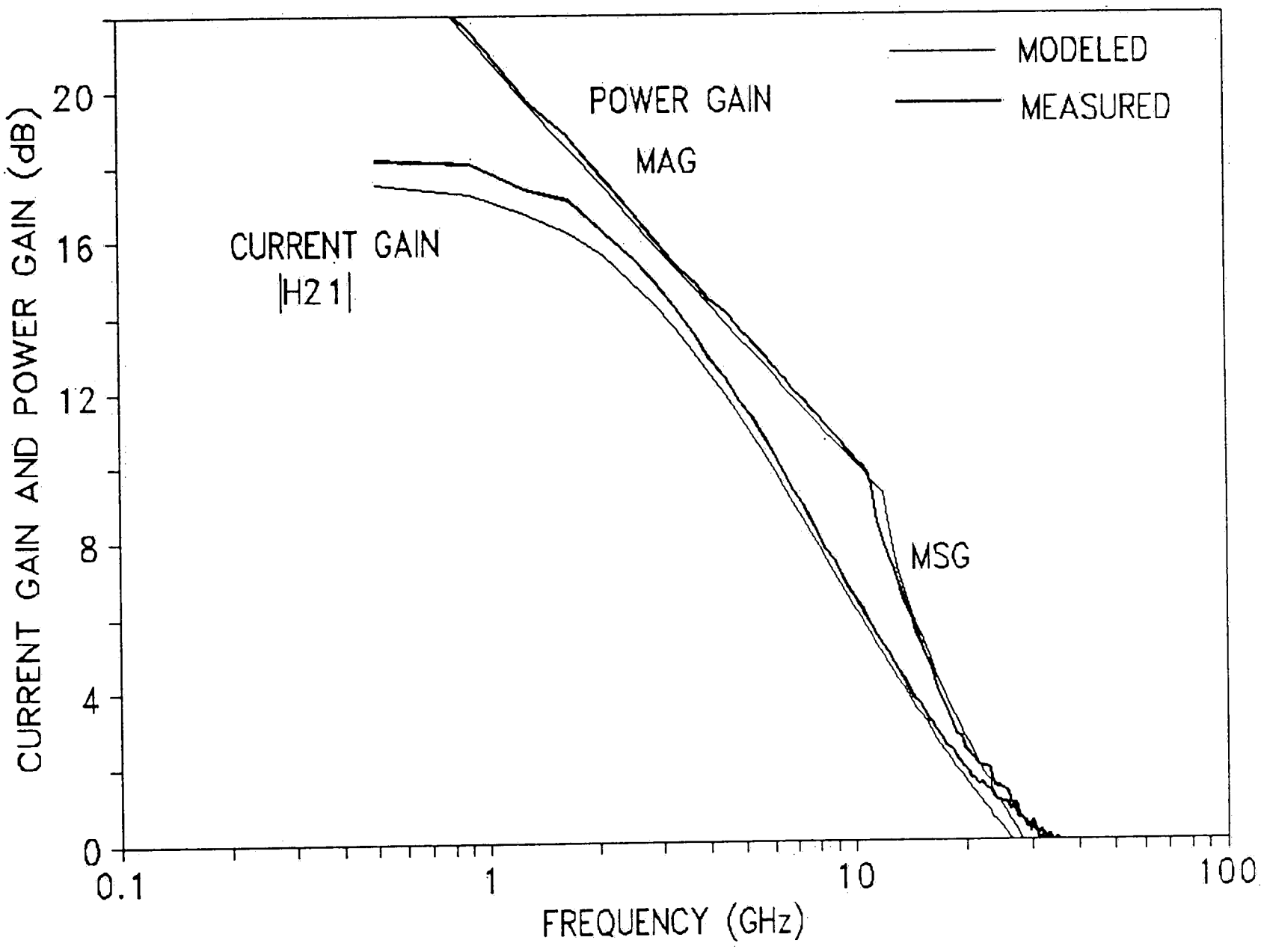

Figure 25. Modeled versus measured current and power gains.
Forward current gain (|H21|) and power gain (MAG and MSG) show excellent agreement to measured data.

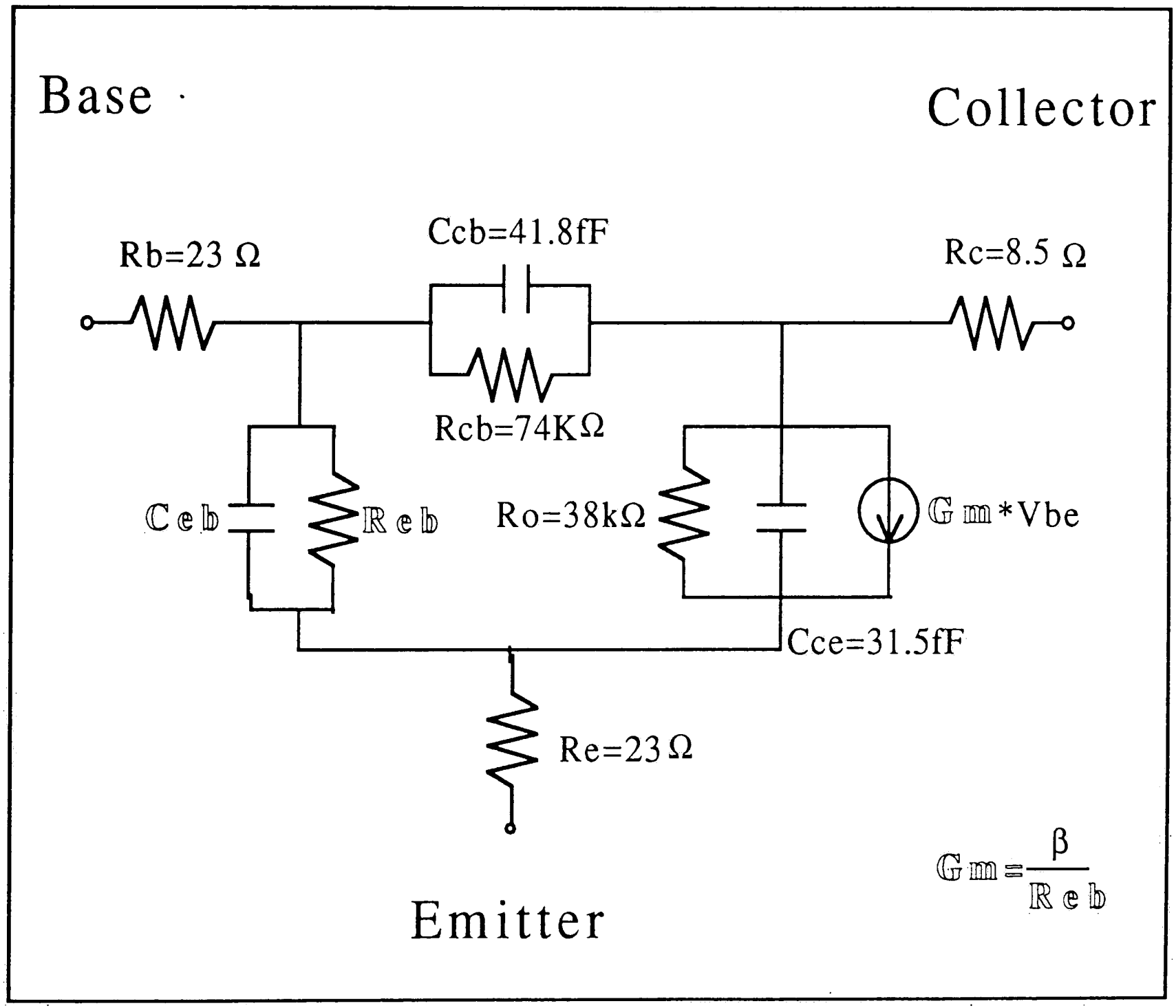

Figure 26. Final bias dependent model with element values.

Reb, Ceb and β are allowed to vary with bias while the remainder of the elements are fixed as noted.

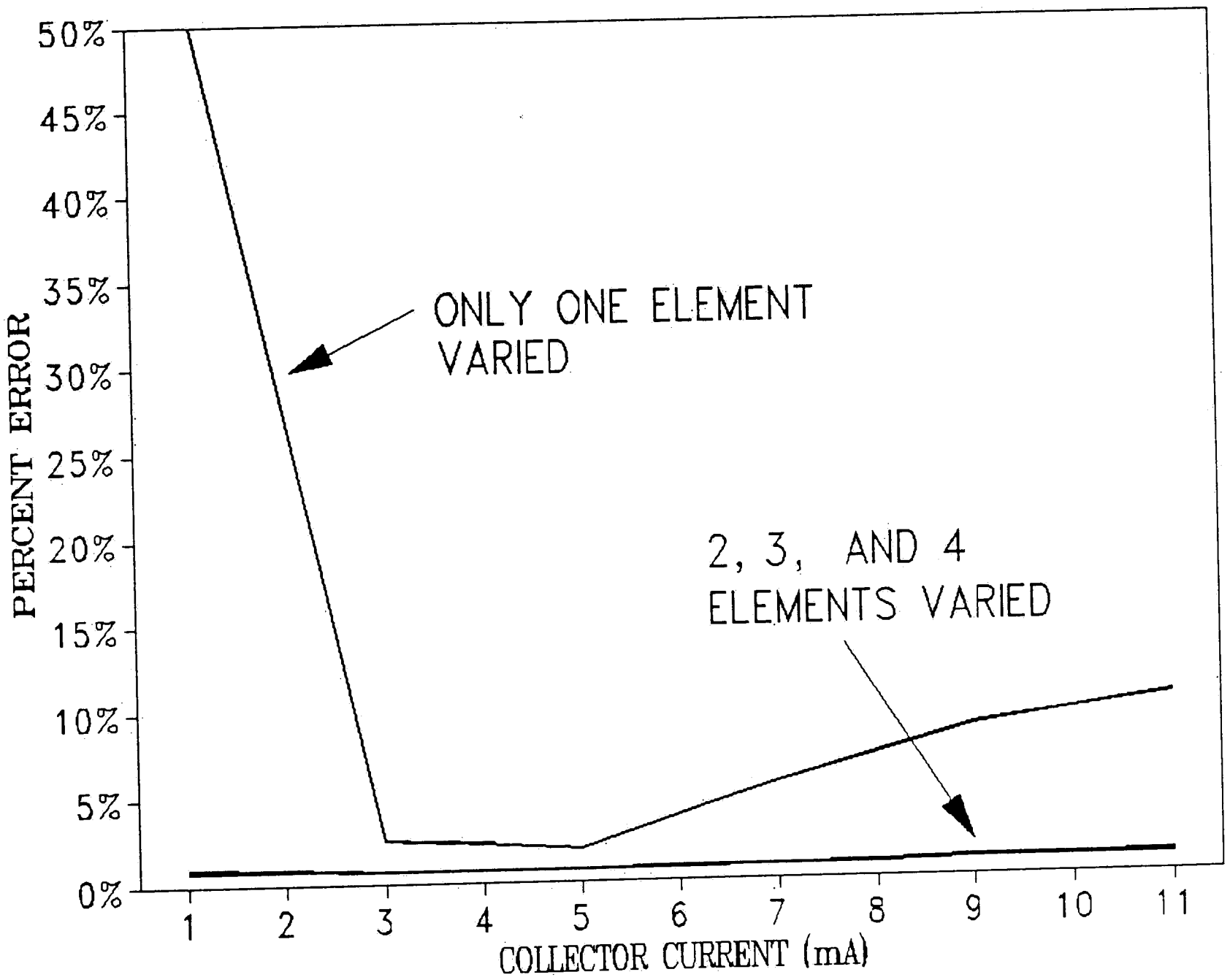

Figure 27. Model error analysis.

The bias dependent model is accurate to less than 2% when two, three and four elements are varied with bias. When only one element is varied the error is unacceptable.

VITA

David S. Whitefield was born in Philadelphia Pennsylvania on December 27, 1967. He attended Lehigh University in 1985 with the support of an Air Force ROTC scholarship. He graduated with high honors in June 1989 with a Bachelor of Science degree in Electrical Engineering and was commissioned a Second Lieutenant in the United States Air Force. He received an educational delay from the Air Force to attend graduate school at Lehigh University. After receiving his MSEE degree in June 1991, Mr. Whitefield will continue at Lehigh University in a doctoral program.